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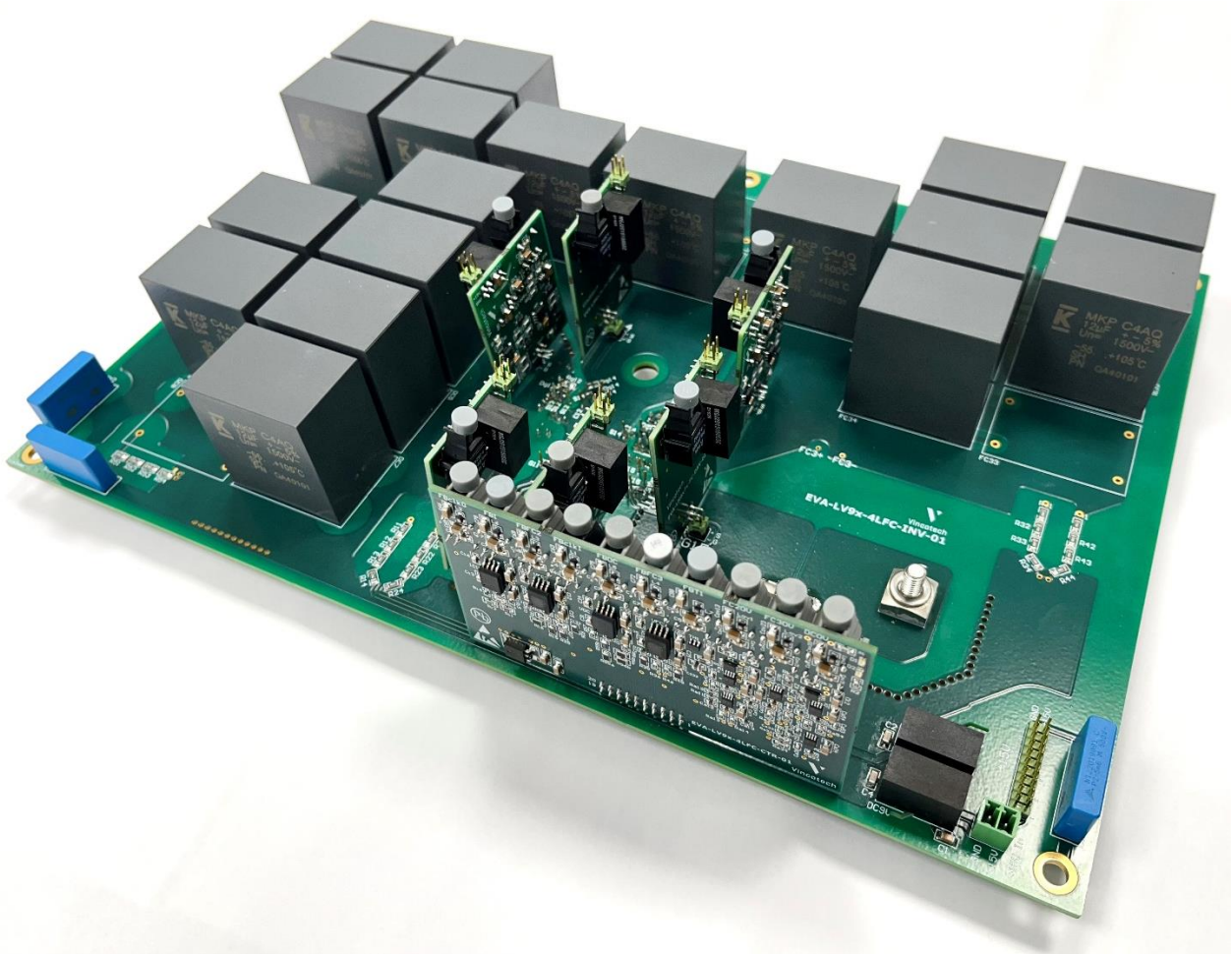
Four Level Flying Capacitor Inverter

Reference Design for flowFC S3 module



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Safety Information

This board classified as an evaluation board (EVA board) dedicated for laboratory environment only. Evaluation board means a product embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes. The board should not be used for reliability testing and may not fulfill all relevant standards and requirements.

This board must be operated by qualified and skilled personnel familiar with all applicable safety standards. Operation must be carried out in a dedicated environment provided with all necessary safety and protective equipments.

This evaluation board contain ESD sensitive parts. Failing to follow the relevant ESD standards may result in device failure and/or even explosion.

This evaluation board operates at high voltages, potentially lethal voltages may be present.

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Please pay attention to the following steps

Before starting the evaluation board please verify that:

- *All parts and components are not damaged or missing.*
- *No conductive foreign objects can be found on the board.*
- *In case of soldering no remaining solder splash can be found on the board.*
- *There is no condensation or water droplets on the circuit board.*
- *All board and cable assembled properly.*
- *The power module is screwed to the heatsink based on FlowS3 handling instruction*

In operation:

- *For optimal thermal behavior, the thermal interface material must be melted (the heatsink temperature must reach at least 45°C)*
- *There is no condensation or water droplets on the circuit board.*
- *Ensure that conductive objects cannot be contacted with the board.*
- *Even brief accidental contact might result in severe injury or death! Therefore, DO NOT touch the board with your bare hands or bring them close to the board.*
- *Be sure to wear insulated gloves when handling is required during operation.*
- *If used under conditions beyond its rated parameters, it may cause defects such as short-circuit or, depending on the circumstances, explosion or other permanent damages.*
- *The heatsink and the board surface may reach high temperatures that might lead to injury, necessary precautions are required*

After operation:

- ***Attention, risk of electrical shock! The voltage of the DC-link always has to be checked before touching the evaluation board!** Since the board contains circuits which stores the electric charges even after the input power are disconnected. Allow at least 4 minutes for the DC-Link and other capacitors to discharge to the safe voltage level (< 50 V).*
- *Please be careful when touching the board or the heatsink. The device can maintain high temperature after switch off, that might lead to burn injury.*

Failure to follow these guidelines may result personal injury or death and/or equipment damage.

Vincotech GmbH is not responsible for any damage caused by use of this evaluation board.

1 Abstract

This application note is intended to describe the EVA-LV9x-4LFC-INV evaluation board as a simplified one phase application example for a three phase four level flying capacitor inverter used in solar applications. To learn more about flying capacitor topology please, visit Vincotech's webpage. https://www.vincotech.com/support-and-documents/technical-library.

2 The power modules

The LV9x family, which is used in this evaluation board, is designed in a way to minimize the commutation loops for superior transient behavior. This is reached by trapezoidal pin-arrangement, where all commutating pins are located as close to each other as possible. The commutation loops of the four-level flying capacitor topology can be seen in Figure 1. So, for the outer commutation loop (blue) the DC+, FC2+, FC2- and DC- pins are in trapezoidal arrangement, while for the middle commutation loop (orange) the FC2+, FC3+, FC3- and FC2- pins are located as close as possible. For the inner loop (green) only the FC3+ and FC3- pins need to be close to each other. The transient behavior is also enhanced with integrated ceramic capacitors in the DC (C10), FC2 (C20) and FC3 (C30) positions. On the other hand, external capacitors still have to be used for the proper behavior. This all results in extremely low module inductance and shorter commutation loops.

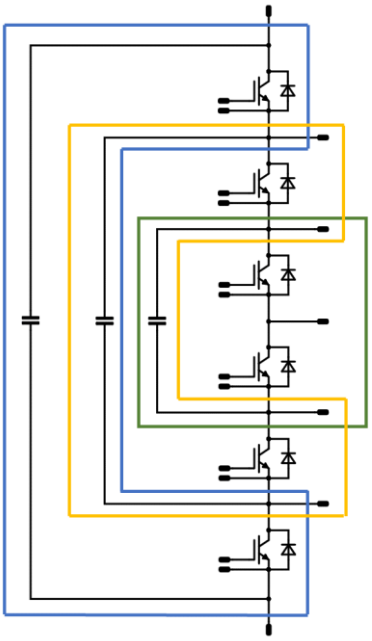


Figure 1 Commutation loops of 4-level FC inverter

The module is using Vincotech's new *flow* S3 low inductive mid-power housing with enhanced thermal performance. For more information about *flow* S3 housing please visit Vincotech's website. https://www.vincotech.com/support-and-documents/technical-library: "New flow S3 Mid-Power Package – the Smarter Way".

The outline and the schematics of B0-SP104FA200S5-LV99F58T-/7/ module can be seen in Figure 2.

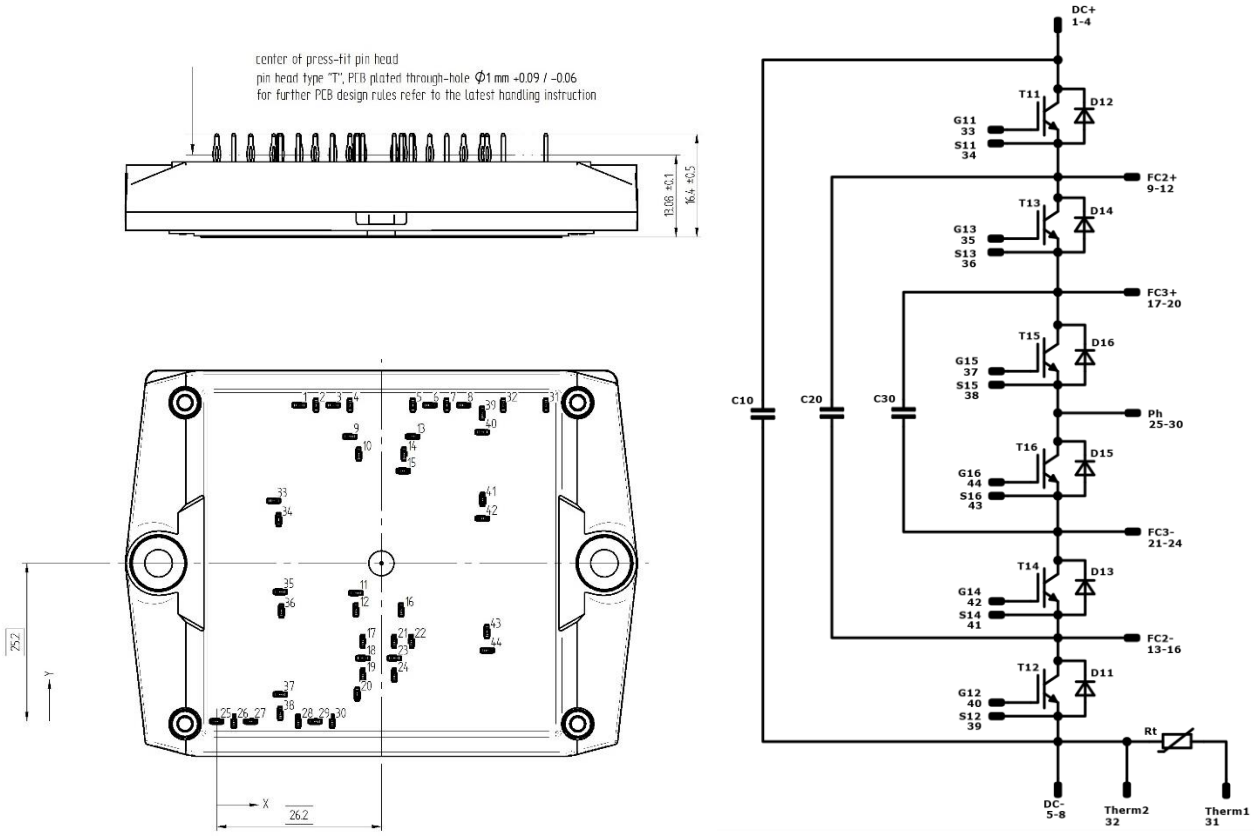


Figure 2 The outline and schematic of LV9x

For more information about the module please visit:
https://www.vincotech.com/products.html.

3 Absolute maximum ratings

Symbol	Parameter	Conditions	Value	Unit
V_{DC}	Maximum DC input voltage		1500	V
I_{outRMS}	Maximum RMS output current	T_s = 80 °C, sinusoidal current waveform	70	A
$I_{outPeak}$	Maximum Peak output current	T_s = 80 °C	100	A
$+15\,V$	15 V supply voltage		16.5	V
T_{PCBmax}	Maximum PCB temperature		115	°C

4 The evaluation board

The evaluation board contains three different PCB cards. The drive (DRV) cards are responsible for driving the related IGBTs. As one card is able to drive one IGBT position six DRV card is required for one phase. The control (CTR) card is responsible for the measurements, A/D conversion and contains the protection circuit. The INV card is the motherboard. It contains the flying capacitors, the DC-link capacitor, the power module and the above-mentioned PCBs. Furthermore, the current sensor, the DC/DC converters and the voltage dividers can be also found on it. In this paragraph all sub-circuits will be explained in details. For more information on the used parts please visit the manufacturer's website and check the manufacturer's datasheets.

4.1 The drive (DRV) card

The DRV cards purpose is to drive the switches. The PWM signal is provided on fiber optics. On the input +15 V should be applied. The output drive signal could be either +15/-15 V or +15/0 V. As the DRV card has one channel output six cards are required for one phase.

The input supply voltage is insulated by MGJ2D151505SC DC/DC converter. LED D1 indicates the presence of the +15 V_{sec}. For the insulated drive signal AFBR-2624Z fiber optic receiver is responsible. AFBR-2624Z is working with +5 V DC. Therefore, an LDO (NCP718BSN500T1G) is used.

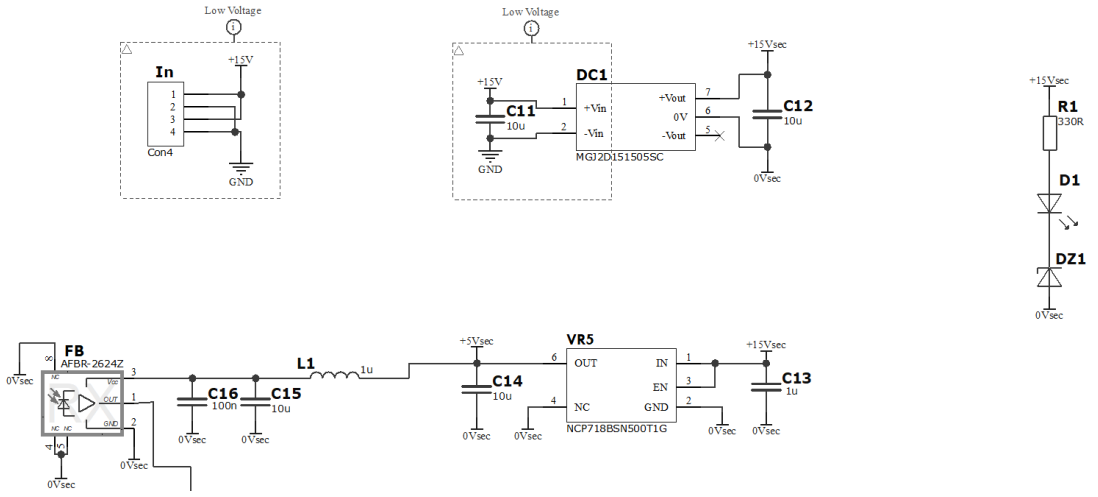


Figure 3 The input part of the DRV card

The output stage is driven by UCC27537 gate driver. The input of the gate drive is filtered by an RC filter to eliminate the noise. Another RC timer is used to provide delay timing for the EN pin. This RC delay and the integrated UVLO protection prevent the unwanted switch ON during start up.

The output stage of the gate driver is a MOSFET H-bridge working with +15 V DC. The gate output is connected to the second half bridge (HB2), while the emitter (source) can be connected by J1 solder jumper either to zero volt or to the first half bridge (HB1). In the first case the output will be +15/0 V, while in the second case +15/-15 V. The default setting for the jumper is the +15/-15 V configuration. The gate output of the DRV card is separated allowing flexible on and off gate resistor usage. Beside the gate resistors two additional resistors (R13, R15) are applied in the gate circuit to reduce the cross-conduction current in the first half-bridge (HB1). The resistance of these two resistors (2 x 100 mΩ) are in series with the gate in case of +15/-15 V configuration and should be taken into consideration during the design. During turn ON R13 increase R_{gon}, while in case of switch OFF R15 increase R_{goff}. On the INV car can be fond a pull-down resistor and a TVS diode as close as possible to the gate protecting it from voltage spikes.

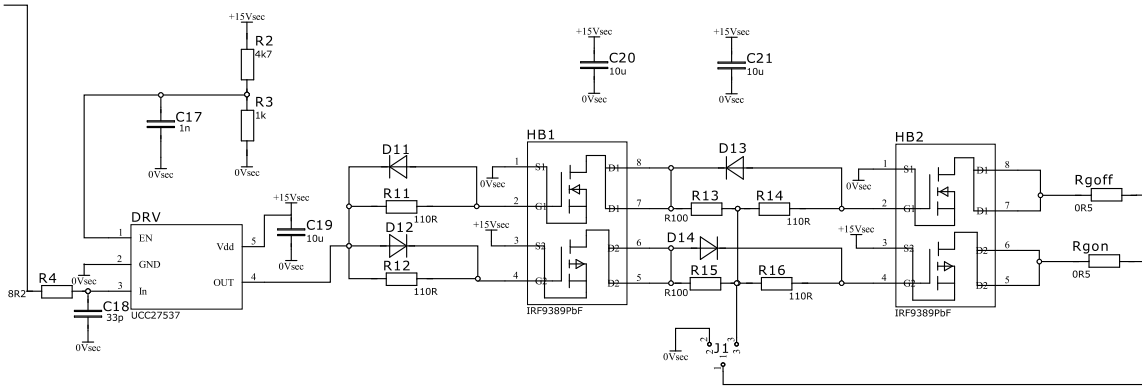


Figure 4 The output stage of DRV card

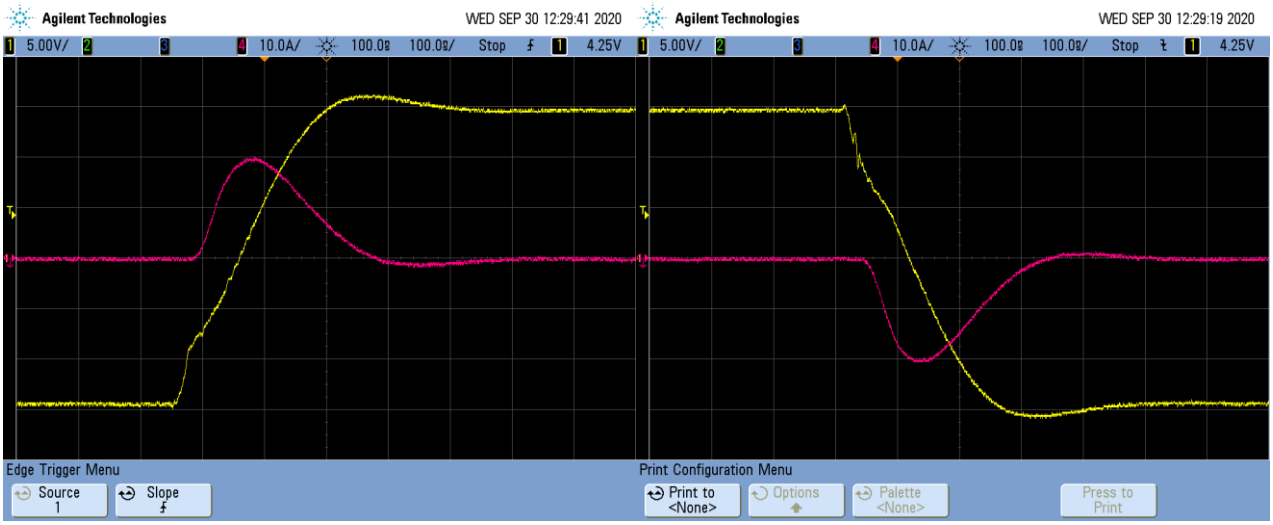


Figure 5 The output of the DRV card (CH1: gate, CH4: output current, J1 is connected to the bridge)

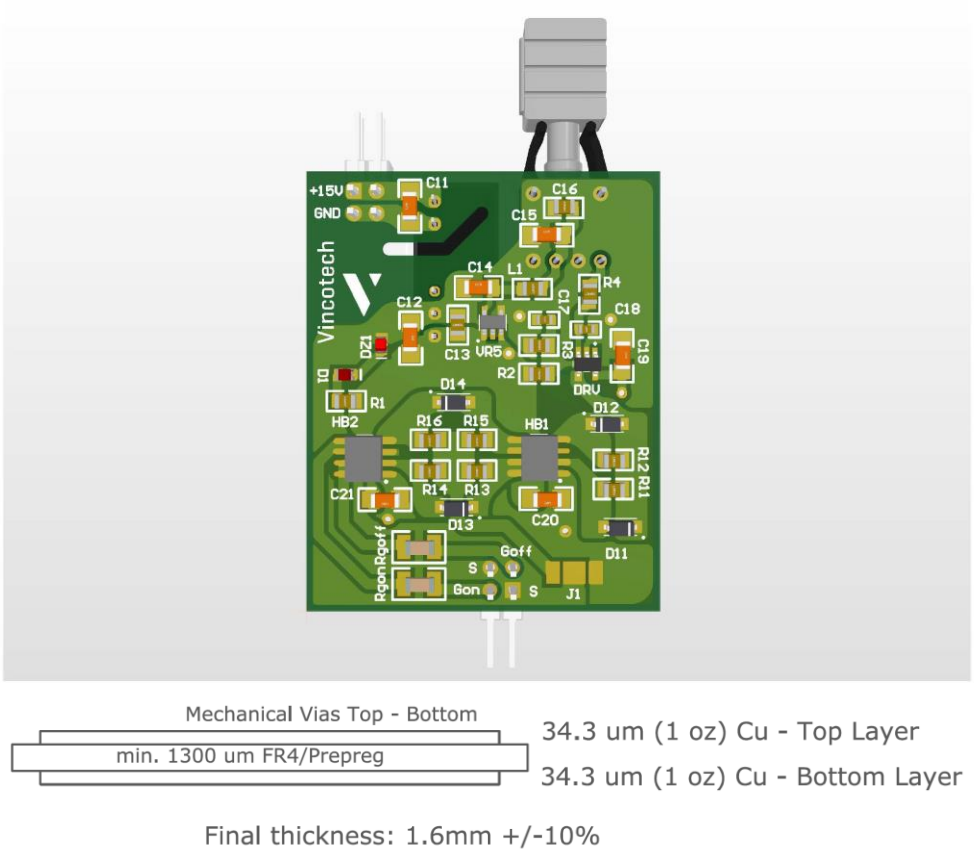


Figure 6 The DRV card

4.1.1 Characteristic Values

T_j = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$+15\,V$	15 V supply voltage		13.5	15	16.5	V
	Symbol rate of the fiber				50	MBd
λ	Optical spectrum of the fiber		630		685	nm
$t_{D_{fiber}}$	Propagation delay of the fiber			30		ns
$t_{r_{fiber}}$	Rise time of the fiber			5		ns
$t_{f_{fiber}}$	Fall time of the fiber			5		ns

$t_{Don_{DRV}}$	Turn-on propagation delay of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		38,4		ns
$t_{Doff_{DRV}}$	Turn-off propagation delay of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		38,2		ns
$t_{r_{DRV}}$	Rise time of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		5,2		ns
$t_{f_{DRV}}$	Fall time of the gate drive circuit	J1 connected to $0V_{sec}$ (1-2), f = 16 kHz, d=0.5		12,4		ns
V_{OH}	High Output voltage of the DRV card			15		V
V_{OL}	Low output voltage of the DRV card	J1 connected to the bridge (1-3)		-15		V
V_{OL}	Low output voltage of the DRV card	J1 connected to $0V_{sec}$ (1-2)		0		V
f_{in}	Input frequency			16		kHz
I_{qu}	Quiescent current	No input is applied		48		mA

4.2 The control (CTR) card

The CTR card is responsible for the voltage, current and thermal measurements, the A/D conversion and the protection of the semiconductors.

For the stable operation an LDO (LDFM50DT-TR) is applied to stabilize the reference voltage for the A/D sigma-delta converters and for the oscillator of the thermistor. LED D1 representing the +5 V, while LED D2 the stabilized +5 V_{stab}.

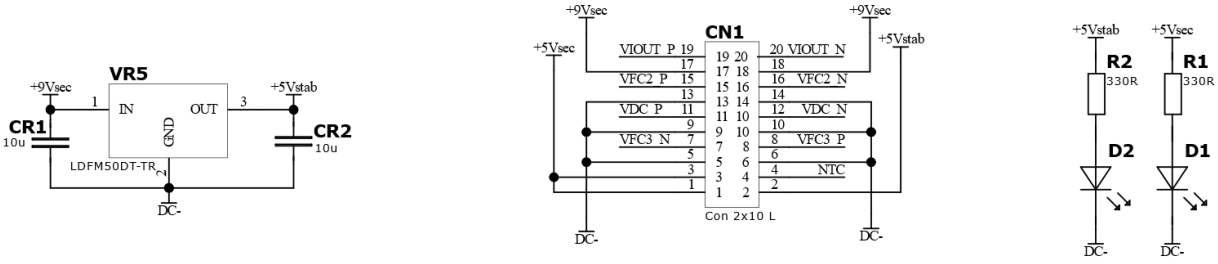


Figure 7 The input connector, the LDO and the LEDs on CTR card

For the flying capacitors and DC-link voltage measurements the voltage divider can be found on the INV card. For A/D conversions high-precision Sigma-Delta converters are used (AMC1336) in case of the flying capacitor voltages, DC-link voltage and the output current. For the reliable operation filters are applied on the input of A/D to reduce both common and differential mode noise. ClkI fiber is the input fiber of the clock signal needed for the Sigma/Delta conversion.

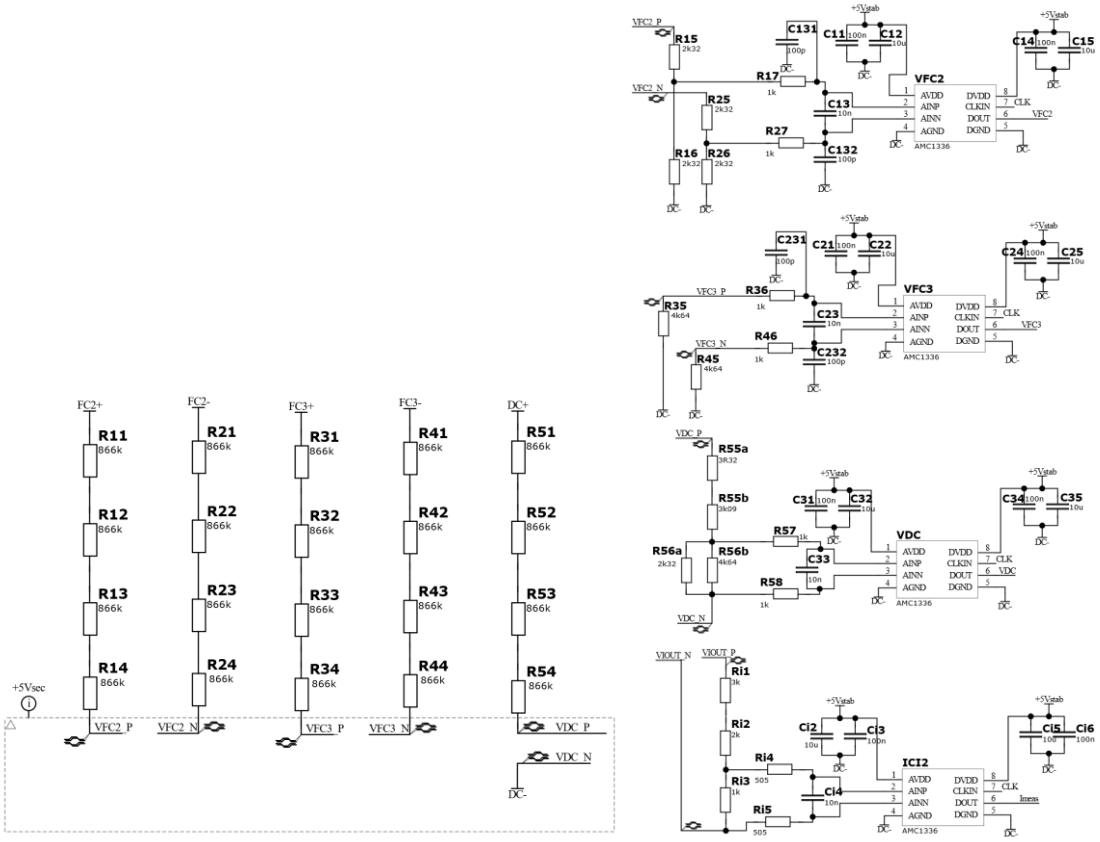
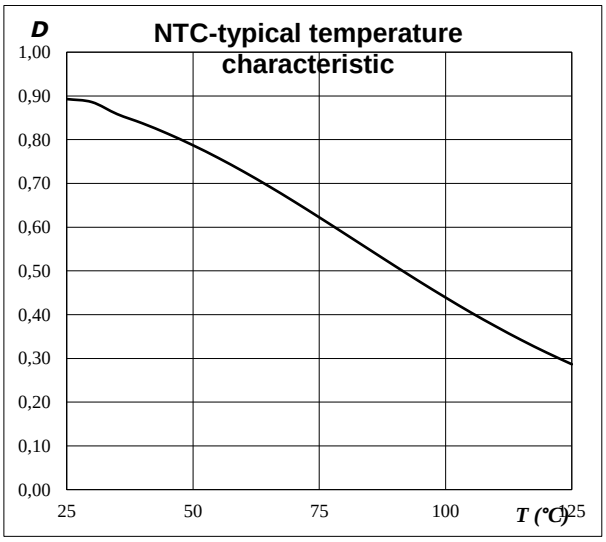


Figure 8 The A/D converters and the voltage dividers (the dividers are located on the INV card)

As this clock signal is in high frequency range, the output of the A/D will be delayed compared to the input clock. Because of this delay the microcontroller could not decode the Sigma/Delta signal. This problem can be solved by ClkO fiber. ClkO transmitter sends back the clock signal to the microcontroller. As this signal will have the same delay as the output data the microcontroller will be able to decode the Sigma/Delta signal with this CLK signal. This delay can be seen on Figure 9.

Figure 9 The delay between ClkI and the received ClkO on the control card on 1,6 MHz and 16 MHz

For the thermal measurement a voltage-controlled pulse width modulator is used (LTC6992-1). The output frequency of the modulator is set to 100 kHz by R51 and R61. As the output duty cycle is controlled by the voltage of MOD pin, the thermistor voltage divider output is connected to that pin. As the NTC changes resistance the output duty cycle will change accordingly. The output duty cycle as function of the temperature can be seen on Figure 10. Please note that if the voltage on the MOD pin is below 5% or above 95% of the supply voltage (+5 V_{stab}), the output duty cycle will be clamped to 0% or 100%.



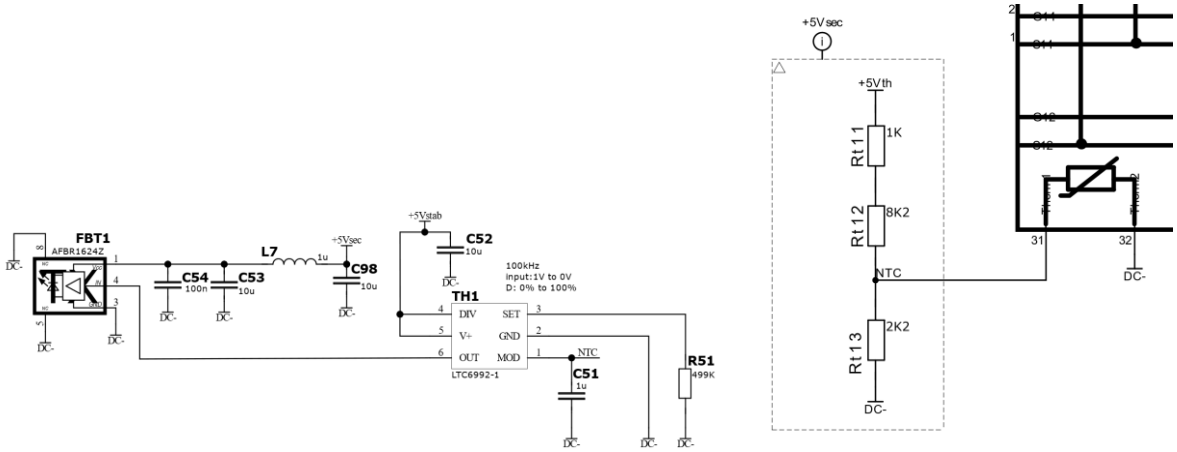


Figure 10 The thermal measurement (The Voltage divider can be found on the INV card)

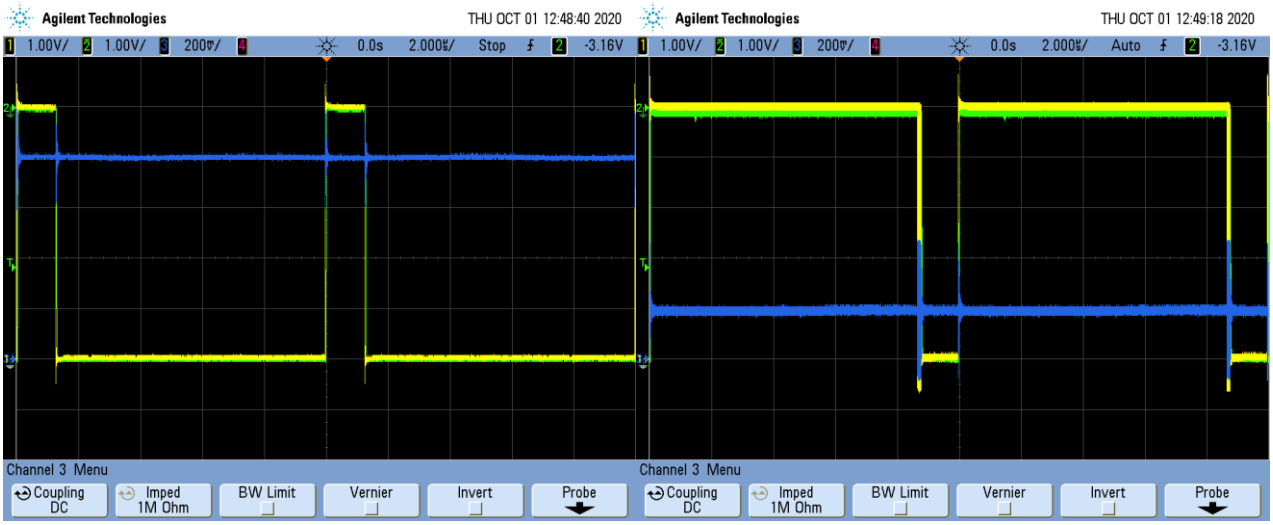


Figure 11 The thermistor output signals (CH1: TH output, CH2: the received signal by the microcontroller, CH3: the voltage of NTC)

The CTR card contains also the flying capacitor protection circuit. This circuit is continuously monitoring all the three commutation loops and detecting over-voltage events. The output of the protection circuit (FC2OV, FC3OV, DCOV) is normally-on. This means in case of a fiber cable failure the inverter will stop preventing damage of the board. In this protection circuit the ADC analog differential amplifier is creating the proportional voltage of the DC-link, while AFC2 of the FC2 capacitor and AFC3 of FC3 capacitor. In the inner commutation loop (T15 and T16) the measured voltage is the same which the semiconductors see. The output of AFC3 amplifier is compared to a constant value by K1 comparator (B channel). If the output of AF3 is higher than the reference voltage the FC3OV output will change the status to zero. In case of the middle commutation loop the semiconductors (T13 and T14) carry the difference of FC2 and FC3 voltage. To create this difference the positive input of A1 differential amplifier is connected to the output of AFC2, while the negative input is connected to AFC3. The output of A1 is compared by K1 comparator to the same value. In case over-voltage is detected FC2OV will go to zero. The outer semiconductors (T11 and T12) see the difference of the DC-link voltage and the outer flying capacitor (FC2) voltage. The difference is created in the same way as in the previous case. The output of ADC and AFC2 is connected to the input of A2. A2 output is compared by K2 comparator to the voltage reference. In case any of the three signals reach the reference value the corresponding fiber (DCOV, FB2OV or FB3OV) will change the status to zero and indicates the overvoltage event to the MCU. This protection should be included on the control side hardware or software. After the safety stop the voltage divider of the pre-charge (will be detailed later) will stabilize the voltage of the flying capacitors. The schematic of the protection circuit can be seen on Figure 12.

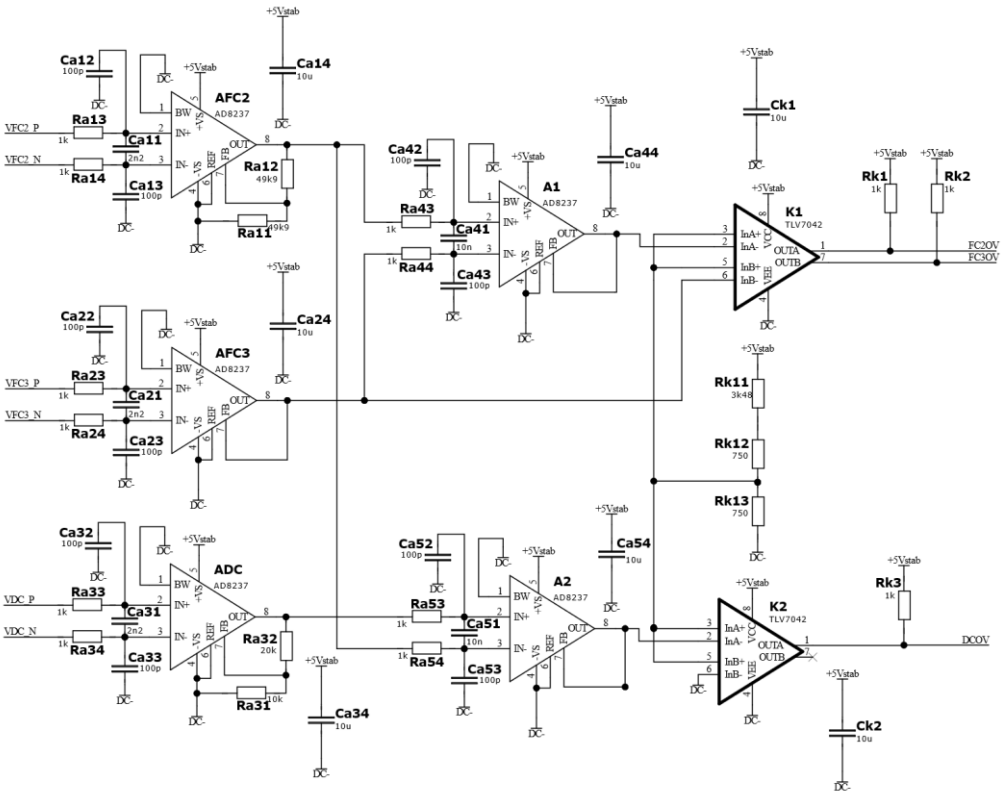


Figure 12 The protection circuit

As the reference voltage is $0{,}753\,V$ and divider creates $1{,}3377\,\frac{mV}{V}$ the protection circuit will change the status at

$$V_{loop} = 562{,}2\,V$$

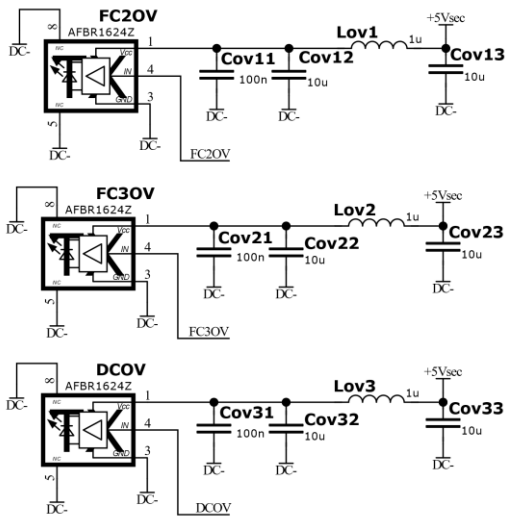


Figure 13 The fibers of the protection circuit

Name	Function
FBclkI	The input clock signal for the sigma-delta converters
FBclkO	The recurring clock signal to eliminate the delay between the incoming and outgoing signal
FBFC3	The inner flying capacitor voltage Σ/Δ converter output
FBFC2	The outer flying capacitor voltage Σ/Δ converter output
FBDC	The DC-link voltage Σ/Δ converter output
$\overline{\text{FB3OV}}$	Protection, overvoltage on the inner flying capacitor
$\overline{\text{FB2OV}}$	Protection, overvoltage on the outer flying capacitor
$\overline{\text{DCOV}}$	Protection, overvoltage on the DC-link
FBI	The output current Σ/Δ converter output
FBT1	The output of the temperature reference

Table 1 The fibers of the CTR card

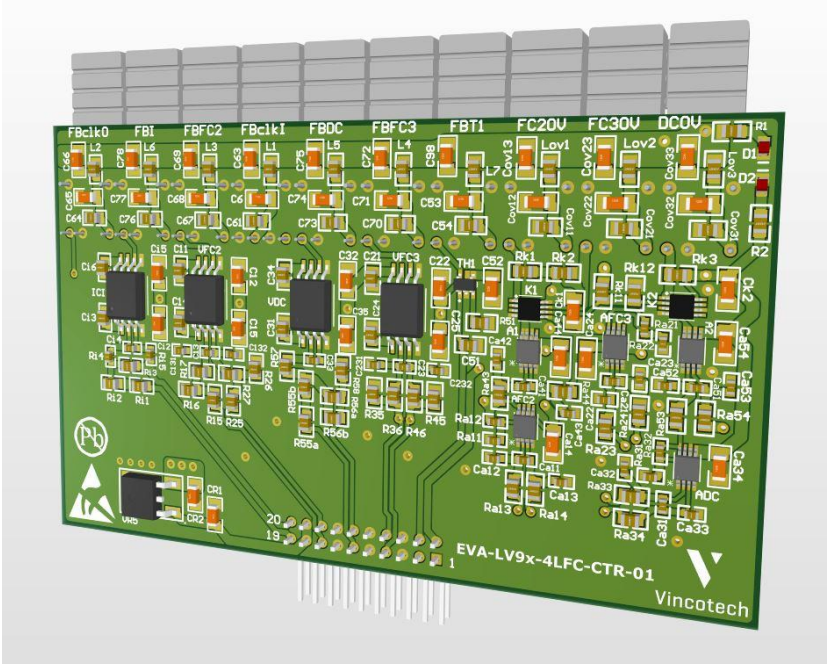


Figure 14 The CTR card

4.2.1 Characteristic Values

T_j = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Y_{DCdiv}	Ratio of the DC-link divider			0,4459		mV/V
Y_{FC2div}	Ratio of the outer flying capacitor divider			0,6689		mV/V
Y_{FC3div}	Ratio of the inner flying capacitor divider			1,3377		mV/V
Y_{Idiv}	Ratio of the current reference divider			0,1667		mV/V
	Resolution of the A/D		16			Bit

f_{CLK}	Clock frequency for the A/D		9	16,6	21	MHz
D_{CLK}	Duty cycle of the CLK for A/D		40%	50%	60%	
f_{FBT}	Output frequency of temperature reference signal			100		kHz
$t_{D_{fiber}}$	Turn-on propagation delay of the fiber			30		ns
$t_{r_{fiber}}$	Rise time of the fiber			5		ns
$t_{f_{fiber}}$	Fall time of the fiber			5		ns

4.3 The inverter (INV) card

The INV card is the mother board of the inverter. The power module, the flying and DC-link capacitors, the DRV and CTR cards, the current sensors, the voltage dividers, the pre-charge resistors, the Y-capacitors and the insulated DC/DC converters are assembled on the INV card. The three Y-capacitor are used to reduce EMI noise and peak voltages between the DC+, DC-, GND, and the heatsink (called GND2 on the schematic).

From the incoming +15 V two insulated DC/DC converter create the secondary voltage levels. One is responsible for the +5 V while the other is for +9 V. The +5 V rail is used for the logical circuits, while from the +9 V rail an LDO (LDFM50DT-TR) creates stable reference for the current sensor.

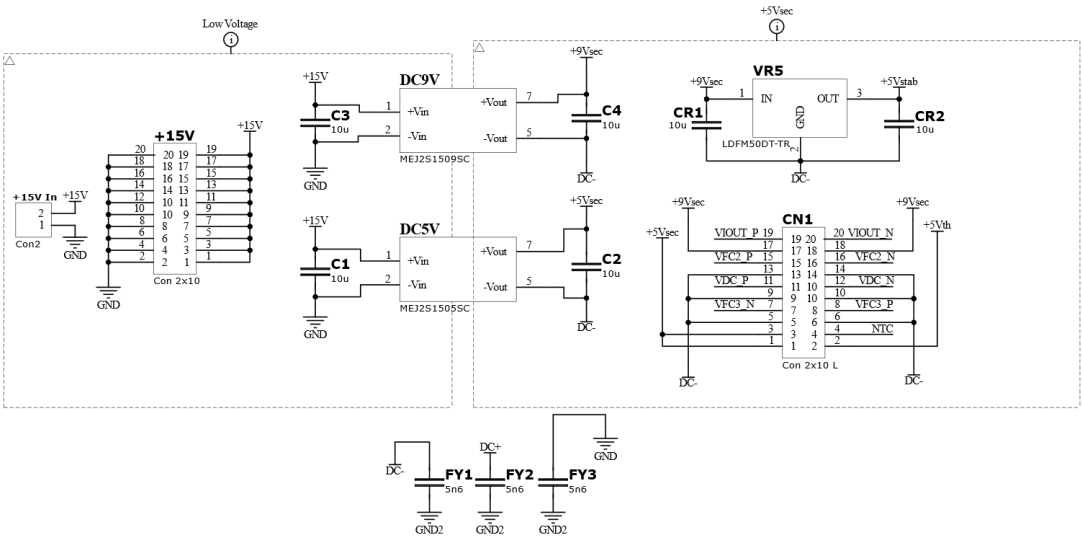


Figure 15 the input stage with the DC/DC converters, the LDO, the CTR card connector and the Y-capacitors

ACS772ECB-200B is bidirectional Hall effect based insulated current sensor. The maximum peak current is +/-200 A, at zero ampere the output of the sensor is 2,5 V.

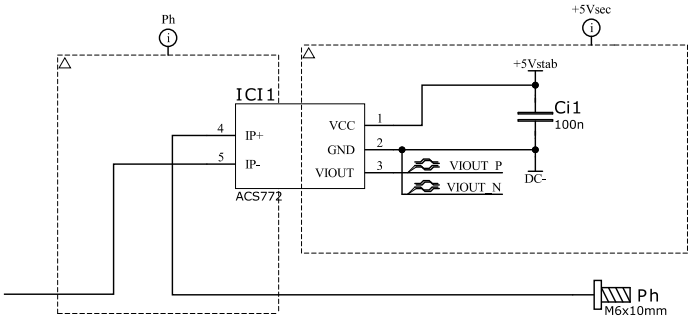


Figure 16 The current sensor

4.3.1 Startup

Before starting up the evaluation board the outer flying capacitor should be charged to the two third of the DC-link voltage, while the inner flying capacitor to one third. This evaluation board uses passive pre-charge circuit for this. A resistive voltage divider is used on the input to charge the flying capacitors to the correct voltage level before startup. As the voltage divider will have a power dissipation during normal operation high resistance values should be used. However, the startup time also depends on the resistance, so the higher the resistance the longer the startup. The voltage divider used for measurement has also an effect for the flying capacitor voltage. This is also balanced by the pre-charge resistors. Please note, that with this

solution the DC-link voltage can be reach the supply value synchronously, while the capacitors need time for charge up. This means as the outer semiconductors are 650 V rated, the DC-link voltage cannot be instantly increased above 1200 V. In case this is needed an additional charging-resistor have to added to the circuit, what should be eliminated (e.g.: with a relay) after start-up. For more detailed description about the pre-charge please check paragraph 3.2 of "The Advantages and Operation of Flying Capacitor Inverter" on Vincotech's webpage.

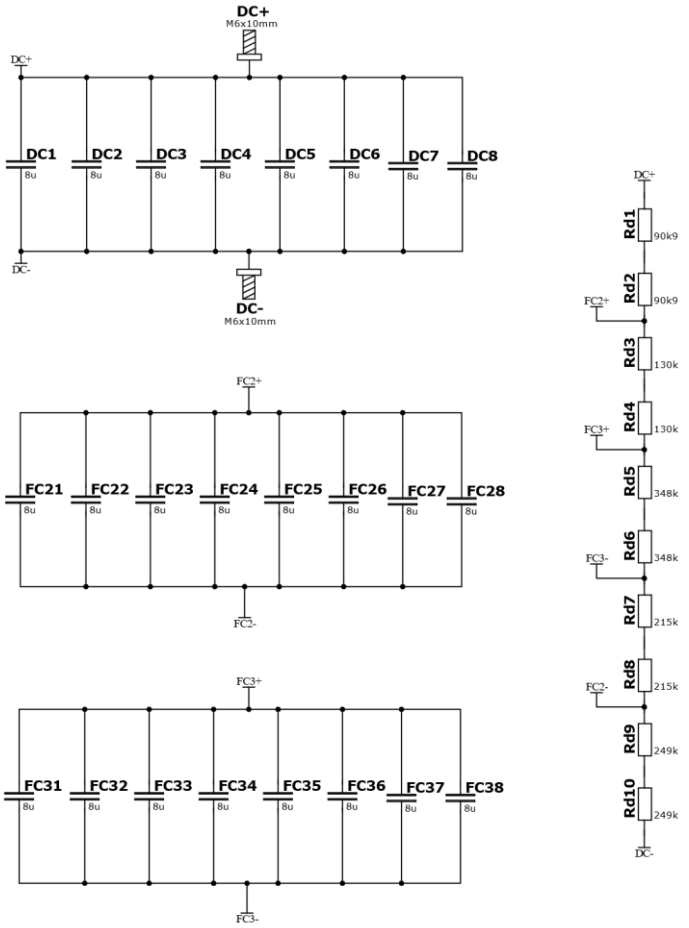


Figure 17 The flying and DC-link capacitors and the pre-charge resistors

4.3.2 Capacitor sizing

The voltage supplied by the flying capacitor has a key role in this topology. To keep the voltage ripple of the capacitor low, suitable capacitor size is needed. To determine the minimum needed capacitance the switching frequency, the output current and the maximum allowed voltage ripple need to be considered. The size of the capacitance can be calculated as:

$$C_{FCmin} = \frac{I_{peak}}{\Delta V_{FC} \cdot 2 \cdot f_{SW}}$$

, where ΔV_{FC} is the maximum allowed voltage ripple, I_{peak} is the maximum current, f_{SW} is the switching frequency of the transistors.

For the capacitor sizing not only the needed capacitance, but also the maximum allowed peak and RMS current should be considered. While the ESR and ESL values should be as low as possible. For more details about flying capacitor selection please check paragraph 3.2 of Flying Capacitor Booster on Vincotech's webpage.

4.3.3 Characteristic Values

T_j = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DC}	DC input voltage			1250	1500	V
$+15\,V$	15 V supply voltage		13.5	15	16.5	V
$I_{OUTpeak}$	Peak current of the current sensor		-200		200	A
	Sensitivity of the current sensor	$I_{Opeakmin}<I_o<I_{Opeakmax}$		10		$\frac{mV}{A}$
V_{Iout0}	Zero current output voltage of the current sensor			2,5		V
C_{DC}	DC-link capacitor			72		µF
C_{FC2}	Outer flying capacitor			72		µF
C_{FC3}	Inner flying capacitor			72		µF
V_{CFC}, V_{CDC}	Maximum FC and DC capacitor voltage				1500	V
$V_{ISODC/DC}$	DC/DC isolation voltage				5,2	kV
I_{qu}	Quiescent current	No input is applied		120		mA
I_{qu}	Quiescent current	Only CLK is applied		140		mA

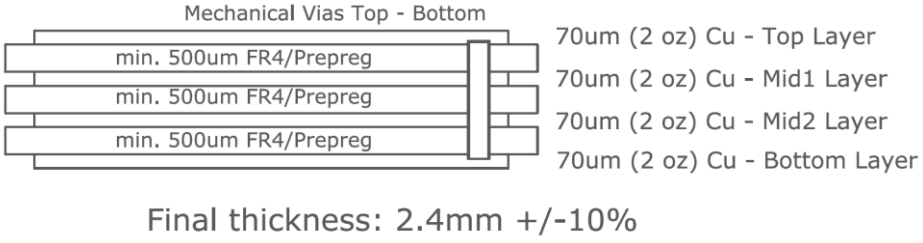


Figure 18 Layer stack of INV card

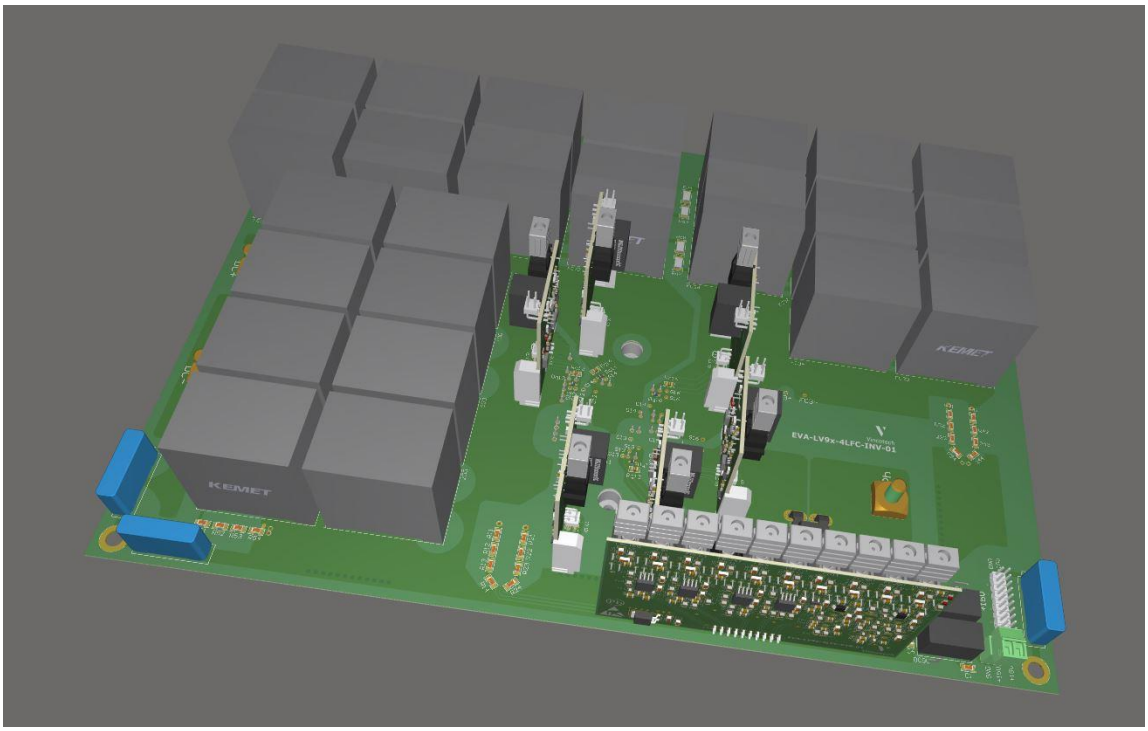


Figure 19 The Evaluation board

4.4 PCB design

To reach optimal switching behavior the PCBs has been designed with the following design criteria. The overlapping layers has been designed to maximize capacitive coupling of the power plane pairs (e.g.: DC+ to DC-, FC2+ to FC2-, FC3+ to FC3-, +5 V_{sec} to 0 V_{sec}) and minimalizing the capacitive coupling to other planes.

On the INV card all high current traces are on two layers to increase the current capability. As outer layers have better thermal properties high current traces are placed both on an outer and on an inner layer to ensure symmetry in of positive and negative feed. FC2-, FC3- and DC- can be found on the top layer and Mid2 layer. While FC2+, FC3+ and DC+ can be found on the bottom layer and Mid1 layer. This alternating arrangement increase the capacitive coupling as well.

The measured signals (except the thermistor) are routed in differential mode. This can eliminate the common mode noise from the measurements. All measured signals are shielded with DC- both on own layer and on the upper and lower layer. The gate potentials are shielded with the emitter potential.

To increase the Creepage distance PCB cutouts are used.

On the inner layers smaller isolation distances can be used. To ensure the insulation capability of the board high voltage test was applied.

5 Flying capacitor balancing

Balancing the flying capacitor has an important role in this topology. For the appropriate operation of the inverter the inner flying capacitor voltage has to be one third of the input voltage, while the outer two third. For the voltage regulation the input voltage, the flying capacitor voltages and the output current direction should be considered. The effect of the possible transistor states as a function of the output current direction can be seen in Table 2.

Output Voltage	Transistors						FC2 voltage		FC3 voltage	
	T11	T13	T15	T16	T14	T12	Positive current	Negative current	Positive current	Negative current
DC+	ON	ON	ON	OFF	OFF	OFF	No effect		No effect	
2/3 DC+	ON	ON	OFF	ON	OFF	OFF	No effect		Increasing	Decreasing
	ON	OFF	ON	OFF	ON	OFF	Increasing	Decreasing	Decreasing	Increasing
	OFF	ON	ON	OFF	OFF	ON	Decreasing	Increasing	No effect	
1/3 DC+	ON	OFF	OFF	OFF	ON	ON	Increasing	Decreasing	No effect	
	OFF	ON	OFF	ON	OFF	ON	Decreasing	Increasing	Increasing	Decreasing
	OFF	OFF	ON	OFF	ON	ON	No effect		Decreasing	Increasing
DC-	OFF	OFF	OFF	ON	ON	ON	No effect		No effect	

Table 2 Output and FC voltage states

The voltage of the flying capacitors can be affected by the different states. For that the PWM signals has to be modified. To change the duration of the different states an offset has to be added to the modulation signal of each commutation loops. To calculate this offset two regulator loops are needed one for each flying capacitor. The input reference for inner regulator loop is $\frac{1}{3} \cdot V_{DC}$, while for the outer $\frac{2}{3} \cdot V_{DC}$. The difference of the reference signal and the feedback signal (the actual voltage of the flying capacitor) is connected to the input of the PI regulator. The output of the PI regulator is the offset what should be multiplied by -1 in case the current direction is negative.

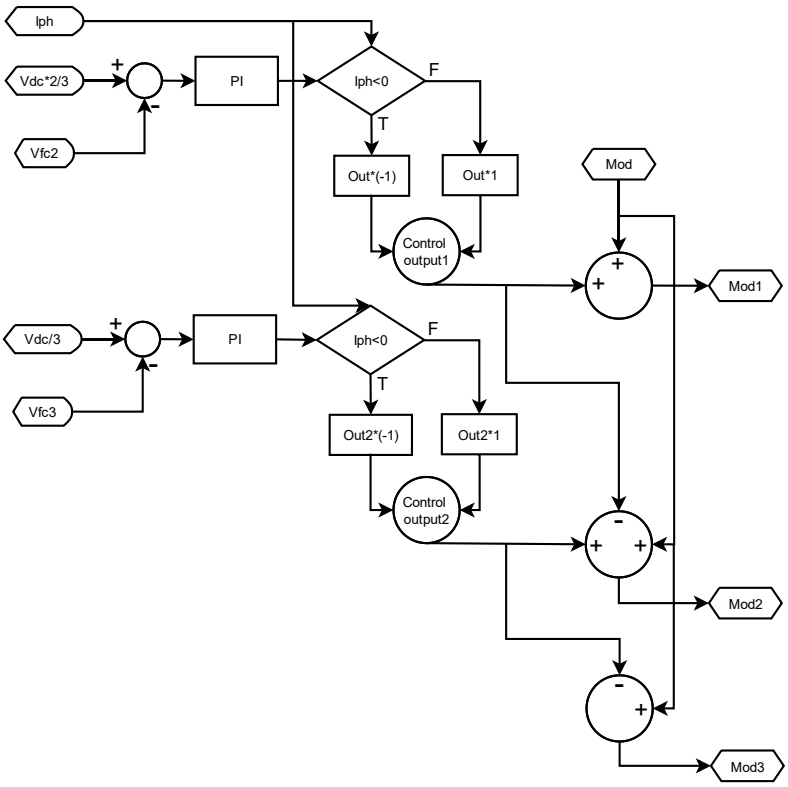


Figure 20 The block diagram of the flying capacitor regulation loops

In general, for every commutation loop, the offset what is calculated from the capacitor which is outside the loop should be subtracted from the modulation base signal, while the offset what is calculated from the capacitor which is inside the loop should be added. This means:

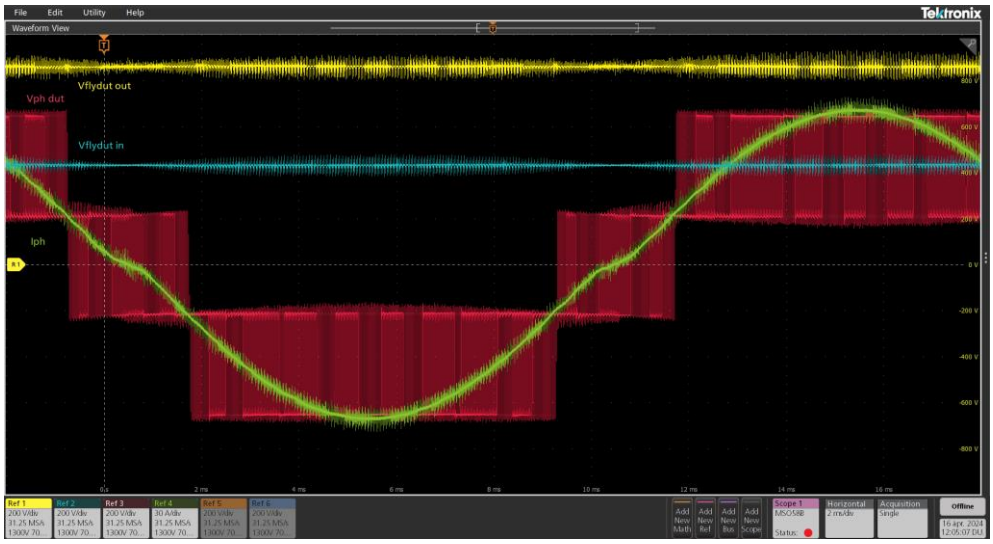
- Outer commutation loop (T11, T12): The offset of VFC2 (control output1) and the modulation base signal (mod) have to be added. The result is the modulation signal (Mod1) of the outer commutation loop.
- Middle commutation loop (T13, T14): The offset of VFC2 (control output1) should be subtracted, while the offset of VFC3 (control output2) should be added to the base signal (Mod). The result is the modulation signal (Mod2) of the middle commutation loop.
- Inner commutation loop (T15, T16): The offset of VFC3 (control output2) should be subtracted from the base signal (mod). The result is the modulation signal (Mod3) of the inner commutation loop.

The block diagram of the four-level flying capacitor regulation loop can be seen in Figure 20.

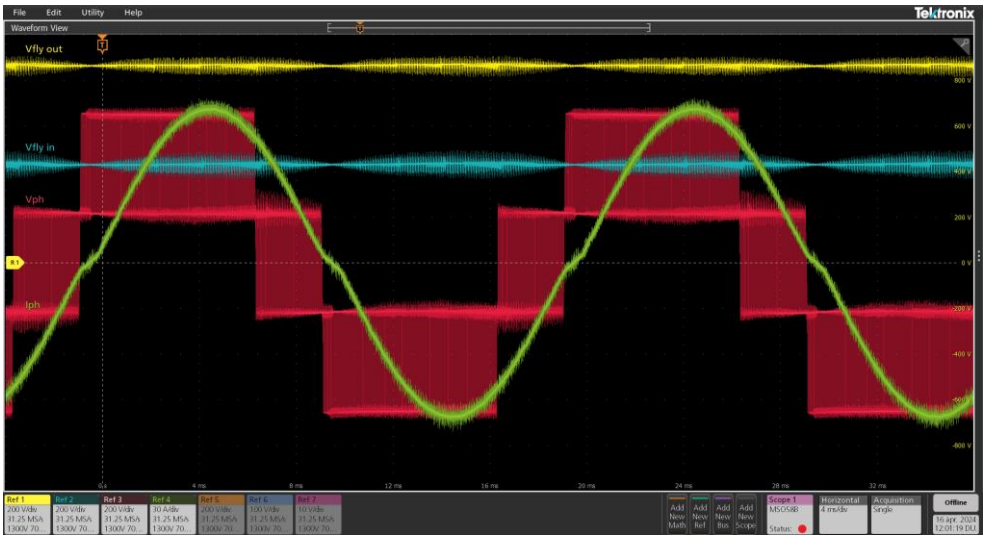
More information can be found about the balancing method of the flying capacitor on Vincotech's web site: The Advantages and Operation of Flying Capacitor Inverter.

6 The measurements of the evaluation board

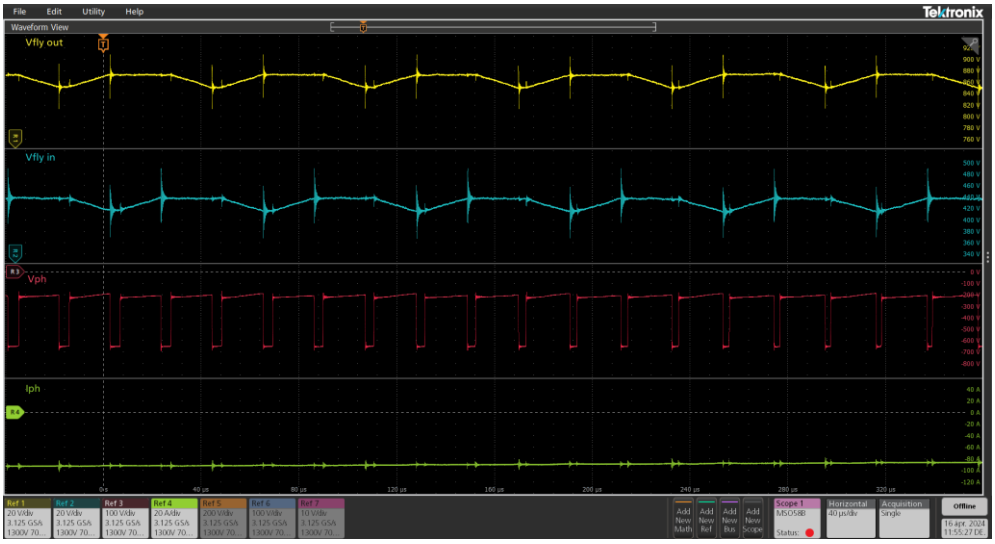
The evaluation board was measured in a single-phase circulator setup. In circulator mode two inverters are connected back-to-back. One of them is the AC power source and the other is the AC power sink. This is an easy way to test more than 26 kW per phase with limited input and output capability in the laboratory. As the measurement only consists of one phase an external DC-link capacitor had to be used. This external capacitor can be eliminated in case three phase system where the input power is constant. The typical waveforms of the evaluation board can be seen in Figure 21.



The output current (Ref 4), the inner flying capacitor voltage (Ref 2), the outer flying capacitor voltage (Ref 1) and the output voltage (Ref 3) at $cos\varphi = 1$



The output current (Ref 4), the inner flying capacitor voltage (Ref 2), the outer flying capacitor voltage (Ref 1) and the output voltage (Ref 3) at $cos\varphi = 0{,}85$



The outer (Ref 1) and the inner (Ref 2) flying capacitor voltage, the output voltage (Ref 3) and the output current (Ref 4)

T16 collector-emitter (Ref 6) voltage, gate-source (Ref 7) voltage and the output current (Ref 4)

Figure 21 Typical waveform of the evaluation board

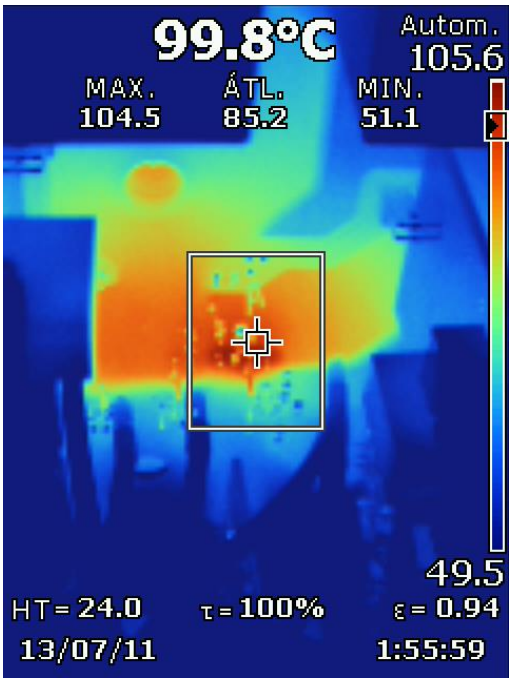
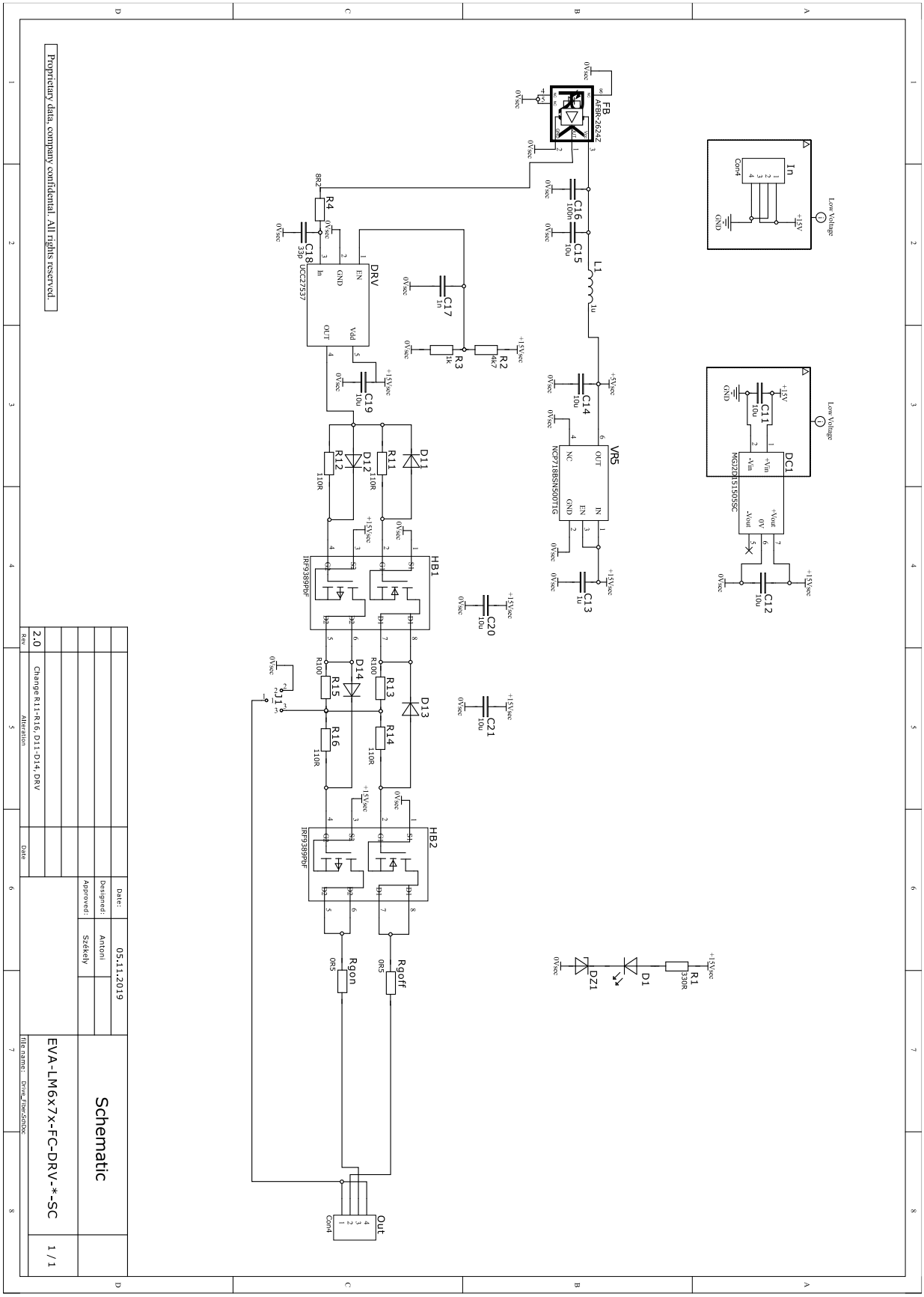


Figure 22 The temperature of the evaluation board during normal operation
($I_{outRMS} = 70\ A,\quad V_{outRMS} = 368\ V,\quad T_s = 80\ °C,\quad T_a = 25\ °C$)

7 Fabrication documents

7.1 Schematics

7.1.1 DRV card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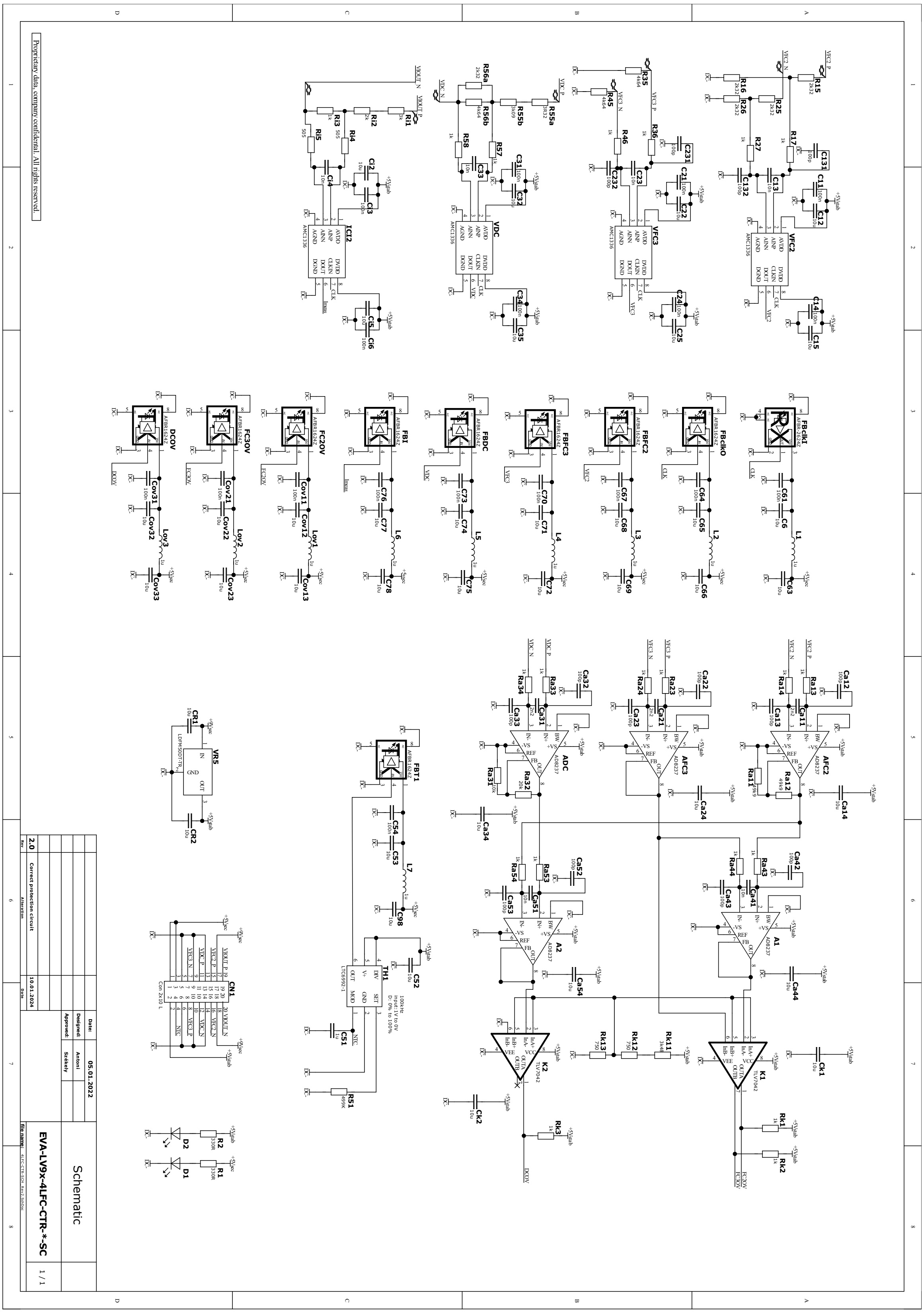
Schematic
EVA-LM6x7x-FC-DRV-*-SC
File name: Drive_FiberSinoc
Designed: Antoni Székely
Date: 05.11.2019
Approved:
Rev. 2.0
Change R11-R16, D11-D14, DRV
Alteration
Date
1 / 1
FB
AFBR-2624Z
In
Com4
GND
+15V
Low Voltage
C16 100n
C15 10u
L1 1u
C14 10u
VR5
NCP718BSN500TTG
C13 1u
C11 10u
DC1
MGJ2D151505SC
C12 10u
R4 8R2
C18 33p
DRV
UCC27537
C17 1n
R3 1k
R2 4k7
C19 10u
D11
D12
R11 110R
R12 110R
HB1
IRF9389PbF
C20 10u
C21 10u
D13
D14
R13 R00
R14 110R
R15 R00
R16 110R
HB2
IRF9389PbF
Rgon 0R5
Rgoff 0R5
DZ1
D1
R1 330R
Out
Com4

7.1.2 CTR card



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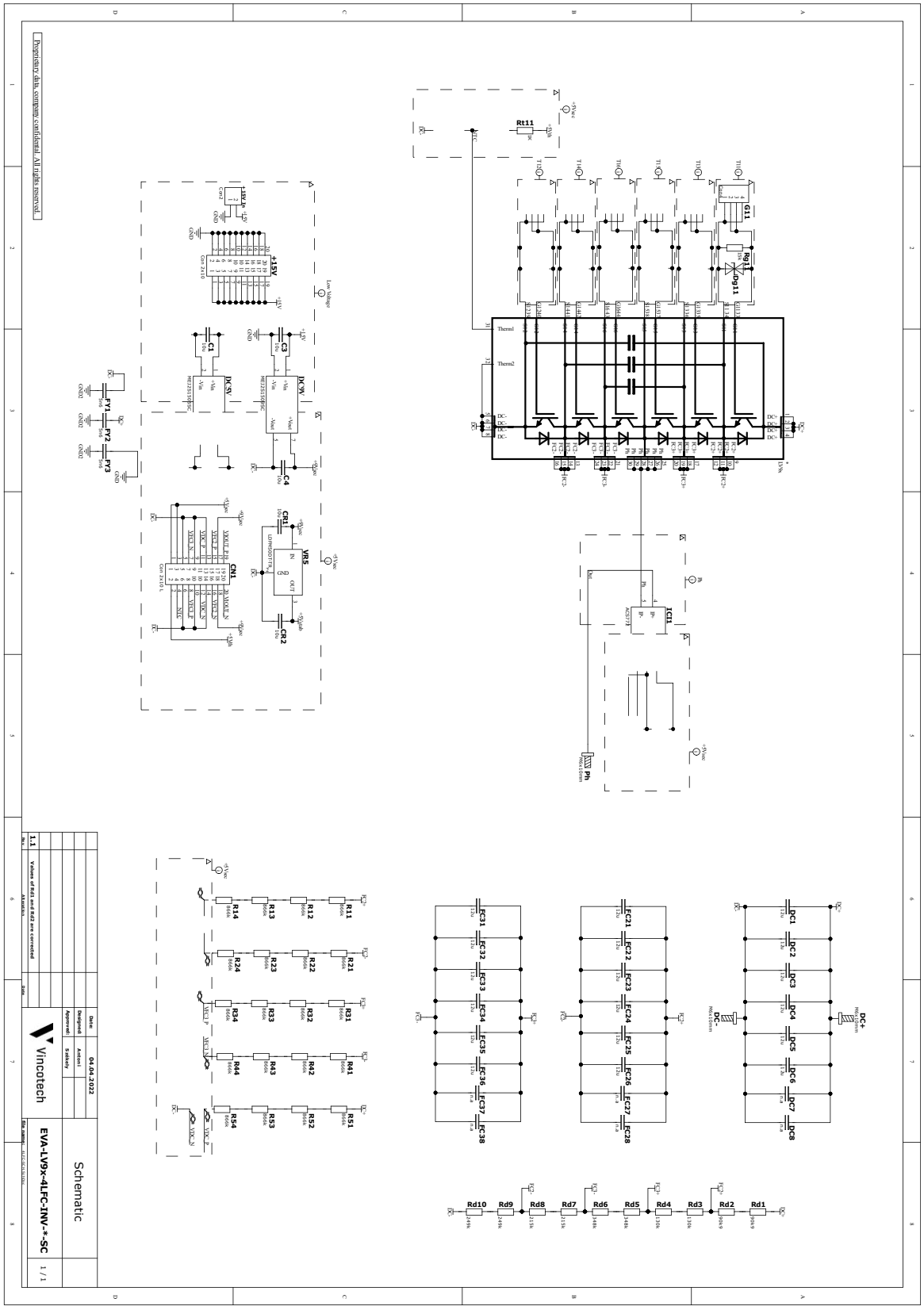
Schematic
EVA-LV9x-4LFC-CTR-*-SC
Correct protection circuit
05.01.2022
10.01.2024

7.1.3 INV card


Proprietary data, company confidential. All rights reserved
Rt11
G11
Dg11
Therm1
Therm2
ICG1
CN1
CN2
VR5
EVA-LV9x-4LFC-INV-*-SC
Schematic
Vincotech
04-04-2022
1 / 1

7.2 BOM

7.2.1 DRV Card

Nr.	Name	Value	Type	Manufacturer	Designators	Qty.
1	Amplifier	10 µF	GRM31CR71E106KA12	Murata	C11, C12, C14, C15, C19, C20, C21	7
2	Capacitor	1 µF	C0805C105K3RAC	Kemet	C13	1
3	Capacitor	100 nF	0805B104K500CT	Walsin	C16	1
4	Capacitor	1 nF	C0603C102K5RACTU	Kemet	C17	1
5	Capacitor	33 pF	C0603C330J3GACTU	Kemet	C18	1
6	LED		MCL-S270GC	Multicomp	D1	1
7	Diode		1N4148W-E3-08	Vishay	D11, D12, D13, D14	4
8	DC/DC	+15/+15;-5 V	MGJ2D151505SC	Murata	DC1	1
9	IC		UCC27537	Texas Instruments	DRV	1
10	Zener	10 V	BZM55C10	Vishay	DZ1	1
11	Fiber		AFBR-2624Z	Broadcom (former AVAGO)	FB	1
12	MOSFET		IRF9389	Infineon	HB1, HB2	2
13	Connector		826953-2	TE Connectivity	In, Out	2
14	Inductance	1 µH	IMC0805ER1R0J01	Vishay	L1	1
15	Resistor	330 Ω	WR08X3300FTL	Walsin	R1	1
16	Resistor	4,7 kΩ	CRCW08054K70FKEA	Vishay	R2	1
17	Resistor	1 kΩ	WR08X1001FTL	Walsin	R3	1
18	Resistor	8,2 Ω	CRCW08058R20JNEA	Vishay	R4	1
19	Resistor	110 Ω	CRCW0805110RJNEA	Vishay	R11, R12, R14, R16	4
20	Resistor	100 mΩ	ERJ-U6SJR10V	Panasonic	R13, R15	2
21	Resistor	500 mΩ	RCWE1210R510FKEA	Vishay	Rgoff, Rgon	2
22	LDO	5 V	NCP718BSN500T1G	Onsemi	VR5	1

7.2.2 CTR Card

Nr.	Name	Value	Type	Manufacturer	Designators	Qty.
1	Amplifier		AD8237ARMZ	Analog Devices	A1, A2, ADC, AFC2, AFC3	5
2	Capacitor	10 µF	GRM31CR71E106KA12	Murata	C6, C12, C15, C22, C25, C32, C35, C52, C53, C63, C65, C66, C68, C69, C71, C72, C74, C75, C77, C78, C98, Ca14, Ca24, Ca34, Ca44, Ca54, Ci2, Ci5, Ck1, Ck2, Cov12, Cov13, Cov22, Cov23,	38

					Cov32, Cov33, CR1, CR2	
3	Capacitor	100 µF	0805B104K500CT	Walsin	C11, C14, C21, C24, C31, C34, C54, C61, C64, C67, C70, C73, C76, Ci3, Ci6, Cov11, Cov21, Cov31	18
4	Capacitor	10 nF	C1608C0G1H103J080AA	TDK	C13, C23, C33, Ca41, Ca51, Ci4	6
5	Capacitor	1 µF	C0805C105K3RAC	Kemet	C51	1
6	Capacitor	100 pF	C0603C101J5GAC7867	Kemet	C131, C132, C231, C232, Ca12, Ca13, Ca22, Ca23, Ca32, Ca33, Ca42, Ca43, Ca52, Ca53	14
7	Capacitor	2,2 nF	C0603C222K5RAC	Kemet	Ca11, Ca21, Ca31	3
8	LED		MCL-S270GC	Multicomp	D1, D2	2
9	Fiber		AFBR-1624Z	Broadcom (former AVAGO)	DCOV, FBclkO, FBDC, FBFC2, FBFC3, FBI, FBT1, FC2OV, FC3OV	9
10	Fiber		AFBR-2624Z	Broadcom (former AVAGO)	FBclkI	1
11	A/D		AMC1336DWVR	Texas Instruments	ICI2, VDC, VFC2, VFC3	4
12	Comparator		TLV7042DGKR	Texas Instruments	K1, K2	2
13	Inductance	1 µF	IMC0805ER1R0J01	Vishay	L1, L2, L3, L4, L5, L6, L7, Lov1, Lov2, Lov3	10
14	Resistor	330 Ω	WR08X3300FTL	Walsin	R1, R2	2
15	Resistor	2,32 kΩ	CRCW12062K32FKEA	Vishay	R15, R16, R25, R26, R56a	5
16	Resistor	1 kΩ	WR08X1001FTL	Walsin	R17, R27, R36, R46, R57, R58, Ra13, Ra14, Ra23, Ra24, Ra33, Ra34, Ra43, Ra44, Ra53, Ra54, Ri3, Rk1, Rk2, Rk3	20
17	Resistor	4,64 kΩ	CRCW12064K64FKEA	Vishay	R35, R45, R56b	3
18	Resistor	499 kΩ	CRCW0805499KFKEA	Vishay	R51	1
19	Resistor	3,32 Ω	CRCW12063R32FKEA	Vishay	R55a	1
20	Resistor	3,09 kΩ	CRCW12063K09FKEA	Vishay	R55b	1
21	Resistor	49,9 kΩ	CRCW060349K9FK	Vishay	Ra11, Ra12	2
22	Resistor	10 kΩ	CRCW060310K0FKEA	Vishay	Ra31	1

23	Resistor	20 kΩ	CRCW060320K0FKEA	Vishay	Ra32	1
24	Resistor	3 kΩ	CRCW08053K00FKEAC	Vishay	Ri1	1
25	Resistor	2 kΩ	CRCW08052K00FKEAC	Vishay	Ri2	1
26	Resistor	505 Ω	RT0603BRD07505RL	Yageo-(Phycomp)	Ri4, Ri5	2
27	Resistor	348 kΩ	CRCW08053K48FKEA	Vishay	Rk11	1
28	Resistor	750 Ω	CRCW08051K50FKEA	Vishay	Rk12, Rk13	2
29	VCO		LTC6992-1	Linear Technology	TH1	1
30	LDO		LDFM50DT-TR	ST Microelectronics	VR5	1
31	PCB		EVA-LV9x-4LFC-CTR-01-PCB			1

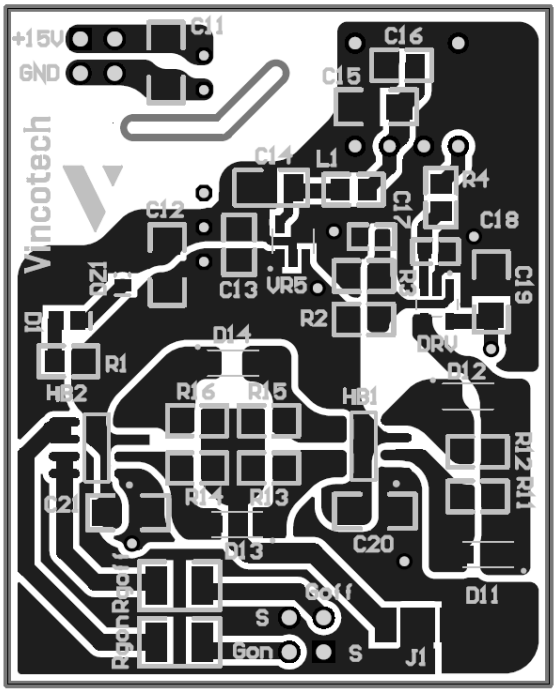
7.2.3 INV Card

Nr.	Name	Value	Type	Manufacturer	Designators	Qty.
1	Power module		B0-SP104FA200S5-LV99F58T-/7/	Vincotech	LV9x	1
2	Connector		1-826632-0	TE Connectivity	+15V	1
3	Connector		MCV 1,5/ 2-G-3,81	Phoenix Contact	+15V In	1
4	Capacitor	10u	GRM31CR71E106KA12	Murata	C1, C2, C3, C4, CR1, CR2	6
5	Capacitor	100n	0805B104K500CT	Walsin	Ci1	1
6	Connector		1-826634-0	TE Connectivity	CN1	1
7	Capacitor	8u	C4AQSLW4800A38J	Kemet	DC1, DC2, DC3, DC4, DC5, DC6, DC7, DC8, FC21, FC22, FC23, FC24, FC25, FC26, FC27, FC28, FC31, FC32, FC33, FC34, FC35, FC36, FC37, FC38	24
8	DC/DC		MEJ2S1505SC	Murata	DC5V	1
9	DC/DC		MEJ2S1509SC	Murata	DC9V	1
10	Connector		7461098	Würth Electronik	DC-, DC+, Ph	3
11	TVS		VLIN1616-02G-E3-08	Vishay	Dg11, Dg12, Dg13, Dg14, Dg15, Dg16	6
12	Capacitor	5n6	B81123C1562M000	TDK	FY1, FY2, FY3	3
13	Connector		826953-2	TE Connectivity	G11, G12, G13, G14, G15, G16	6
14	Current sensor		ACS772ECB-200B-PFF-T	Allegro Microsystems	ICI1	1

15	Resistor	866k	ERJ-P08F8663V	Panasonic	R11, R12, R13, R14, R21, R22, R23, R24, R31, R32, R33, R34, R41, R42, R43, R44, R51, R52, R53, R54	20
16	Resistor	90k	CRCW251290K9FKEG	Vishay	Rd1, Rd2	2
17	Resistor	130k	CRCW2512130KFKEG	Vishay	Rd3, Rd4	2
18	Resistor	348k	CRCW2512348KFKEG	Vishay	Rd5, Rd6	2
19	Resistor	215k	CRCW2512215KFKEG	Vishay	Rd7, Rd8	2
20	Resistor	249k	CRCW2512249KFKEG	Vishay	Rd9, Rd10	2
21	Resistor	15k	CRCW080515K0FKEAHP	Vishay	Rg11, Rg12, Rg13, Rg14, Rg15, Rg16	6
22	Resistor	1K	TNPW08051K00DEEA	Vishay	Rt11	1
23	Resistor	8K2	CPF0805B8K2E1	TE Connectivity	Rt12	1
24	Resistor	2K2	PAT0805E2201BST5	Vishay	Rt13	1
25	LDO		LDFM50DT-TR	Vishay	VR5	1
26	PCB		EVA-LV9x-4LFC-INV-01-PCB			1

7.3 PCB drawings

7.3.1 DRV card



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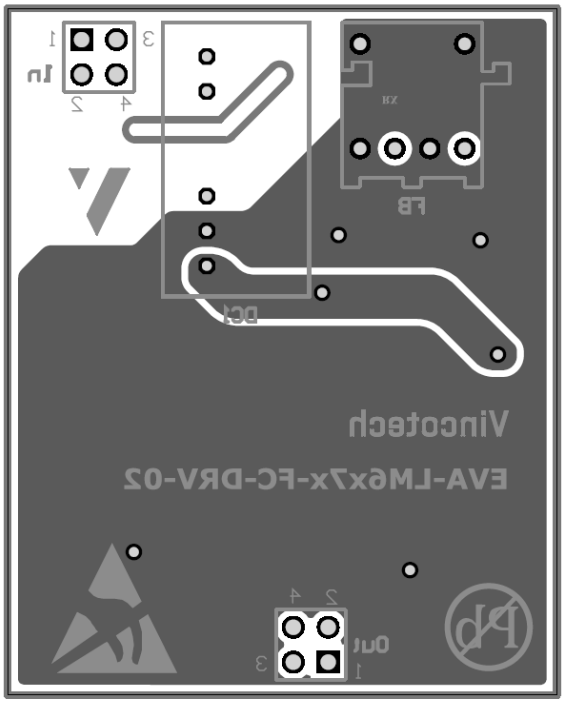
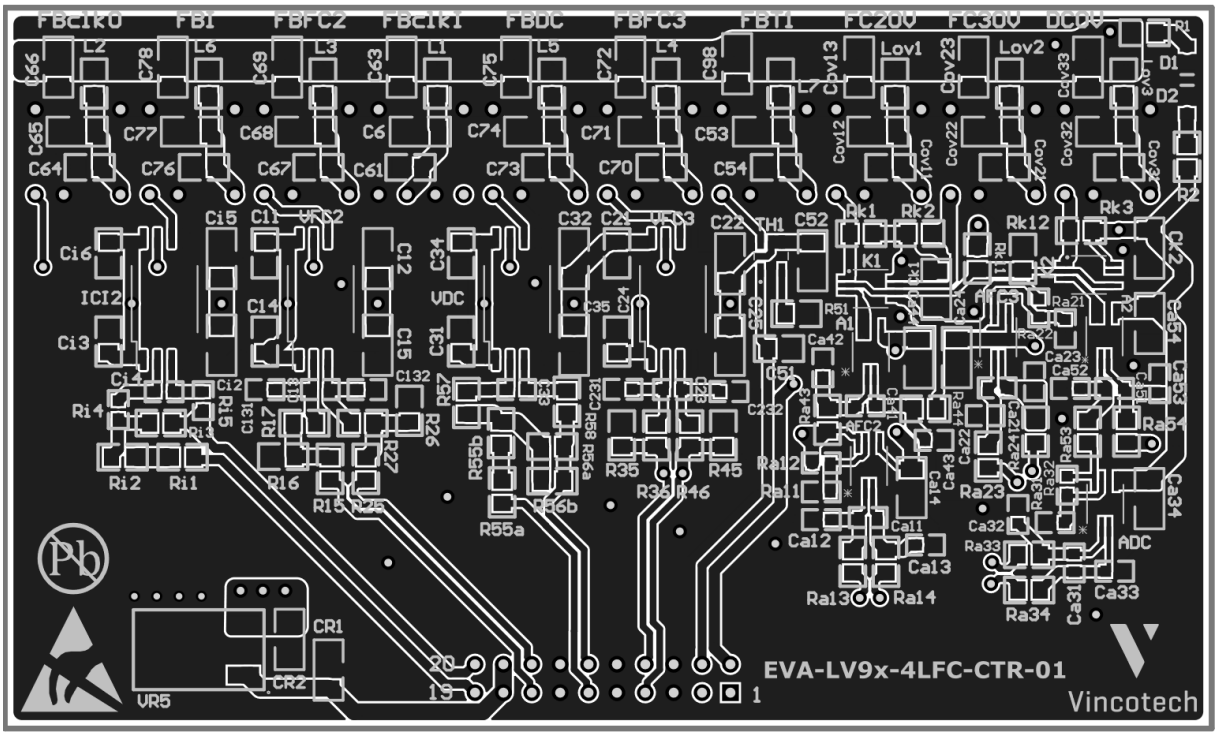


Bottom Layer

7.3.2 CTR Card



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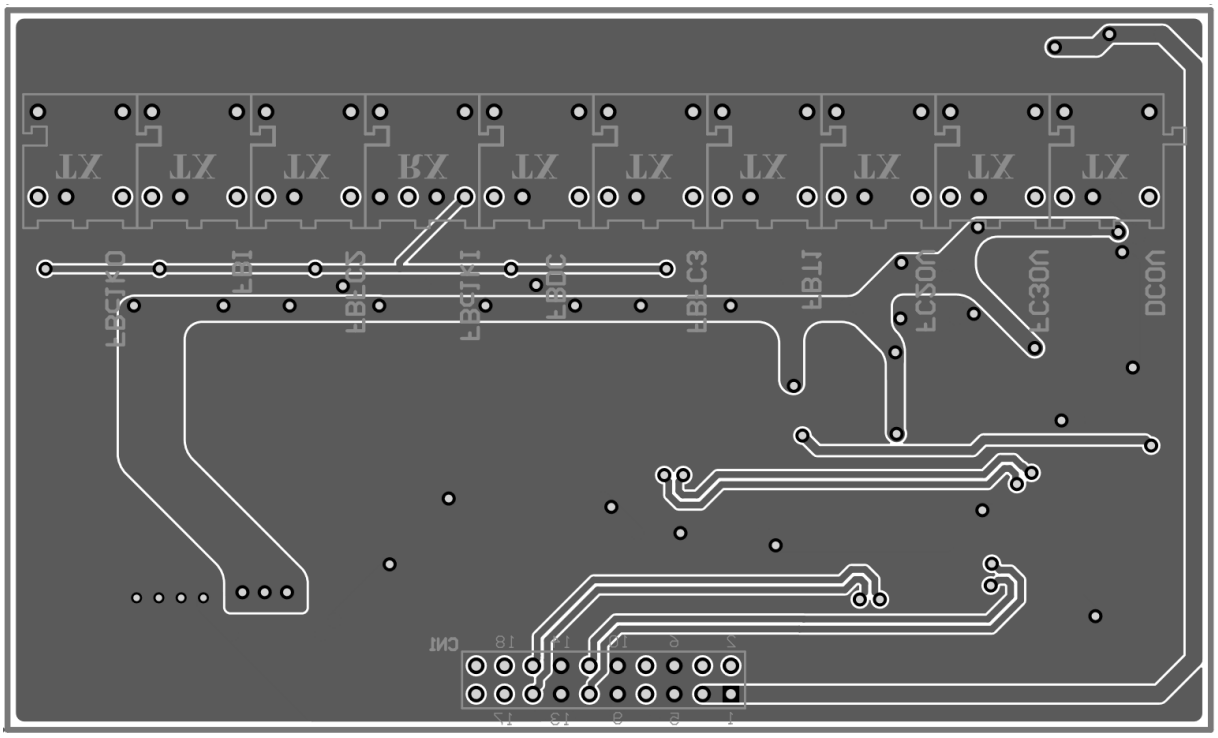

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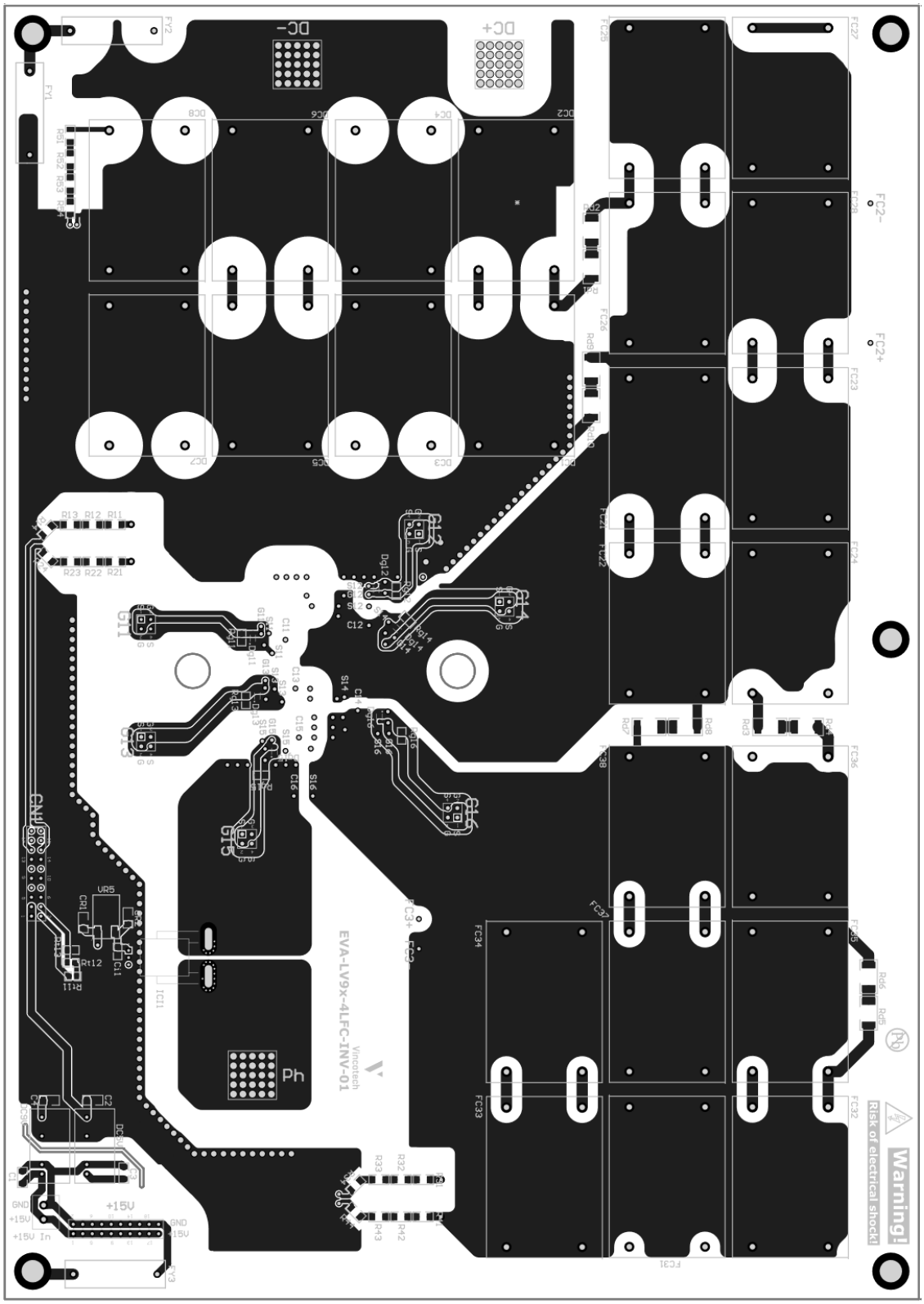
7.3.3 INV card



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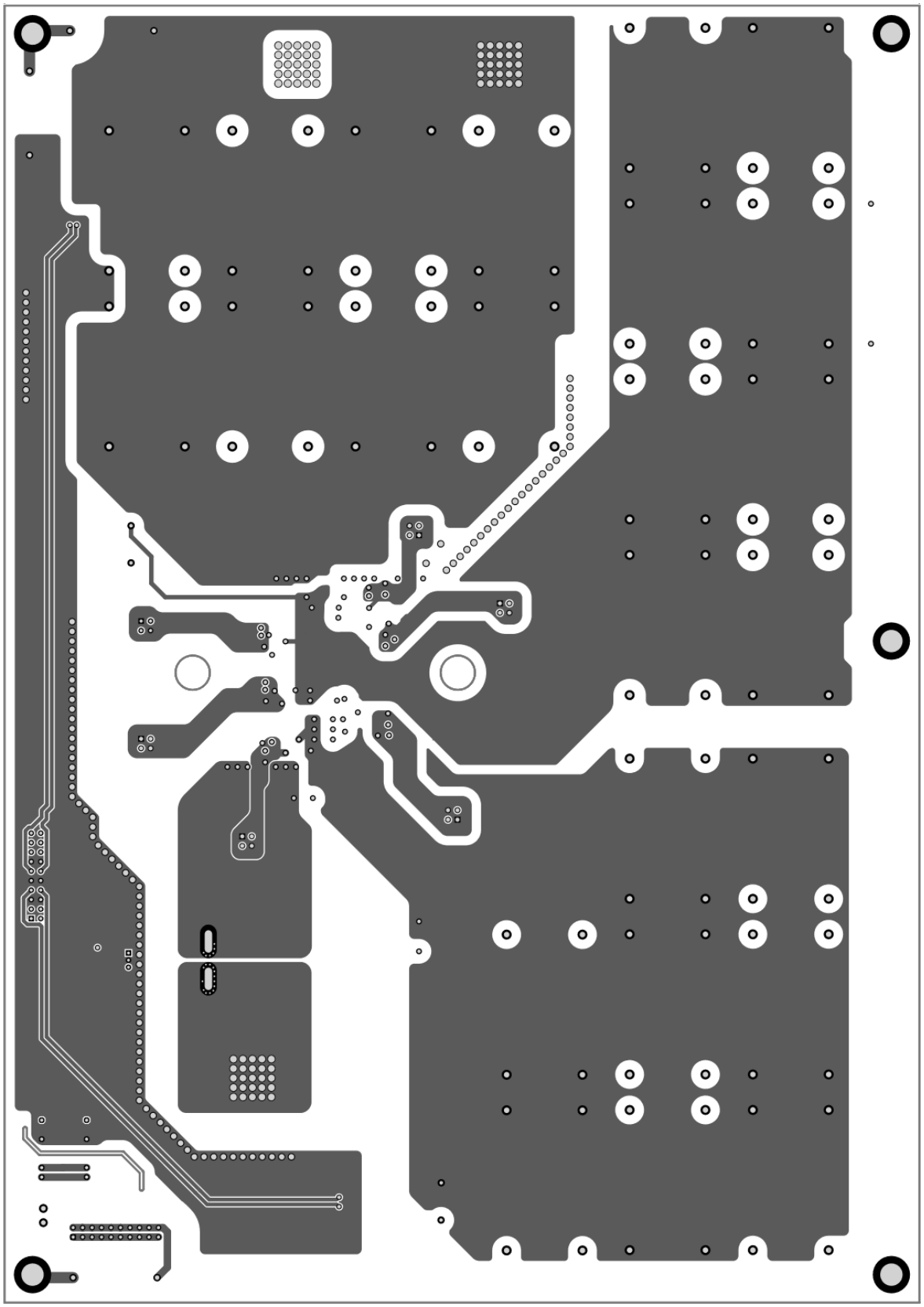
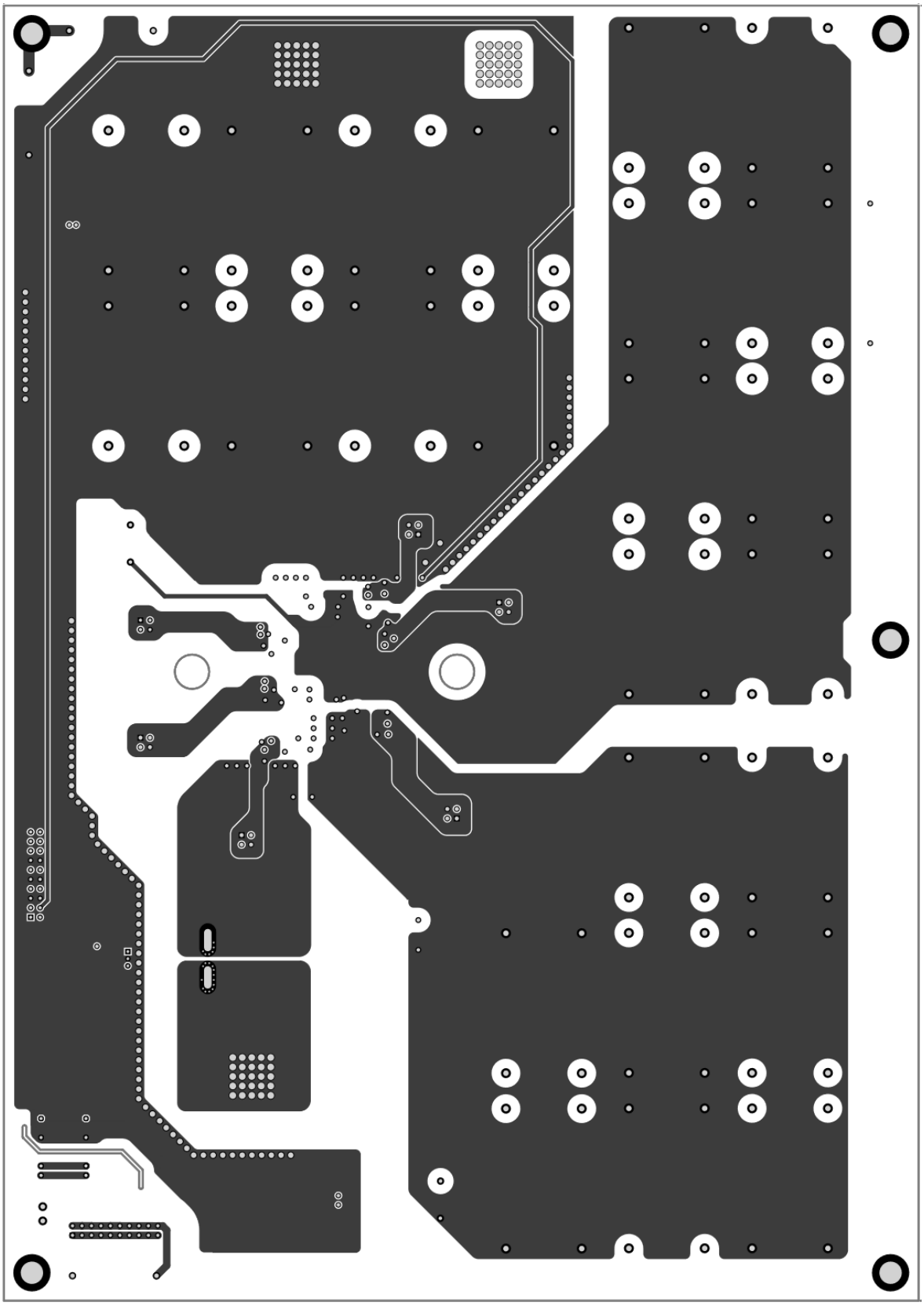
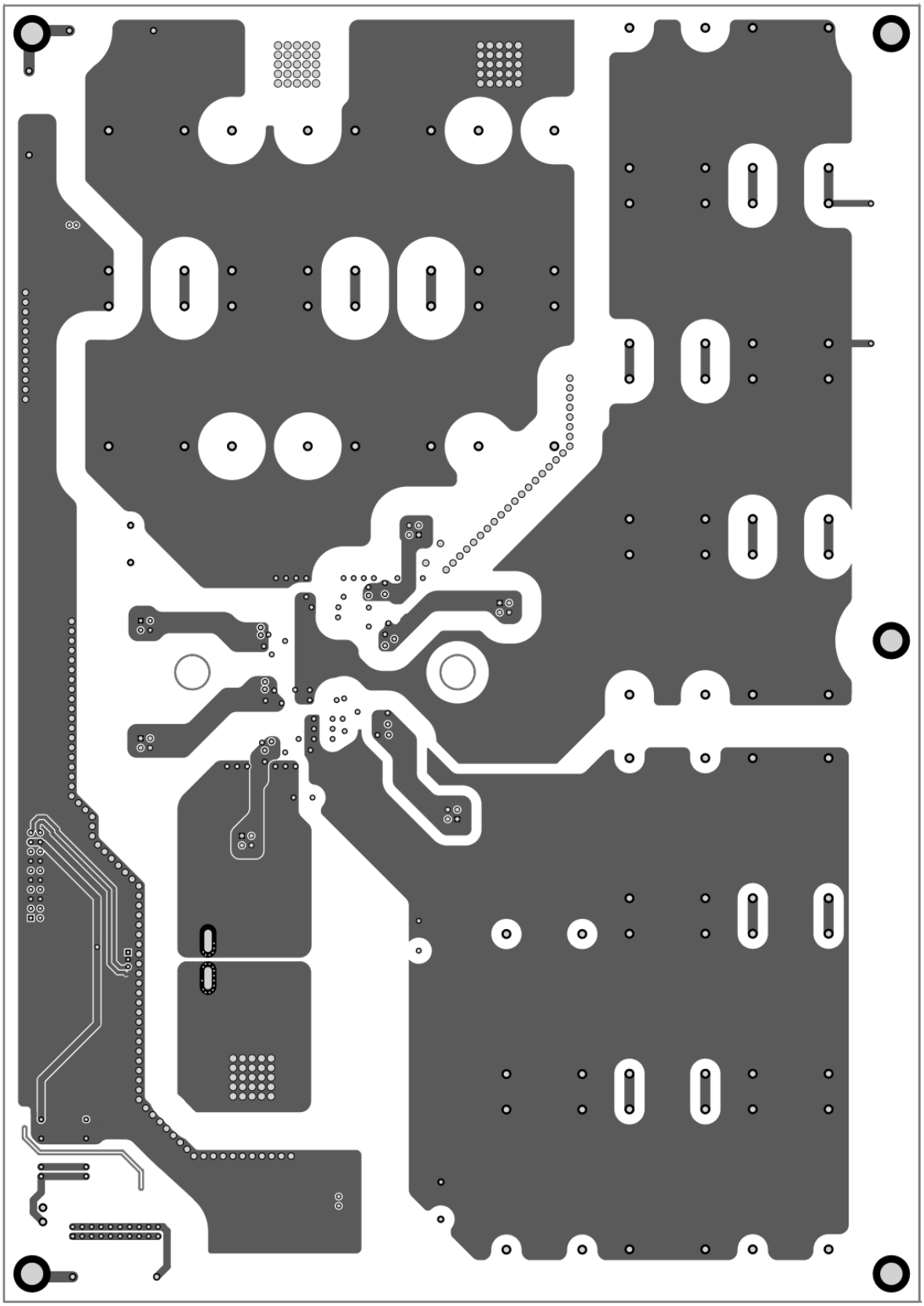


Mid 1 Layer



Mid 2 Layer



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