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Semiconductor Power Losses Reduction Using Tandem Diodes Concepts for Motor Drives Applications

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Abstract

Generally, variable speed motor drives systems use Si-based chipset in standard sixpack topology with switching frequencies up to 16 kHz. Considering filter less implementations between converter and motor, hence, is required that dv/dt-stress on the motor windings should be limited up to 5 V/ns in order to avoid partial discharge phenomena or early insulation failure. The 1200 V pair IGBT and antiparallel freewheeling diode are selected by several figure-of-merit such as cost, efficiency, short circuit capability, EMC and so on. Concurrently, power losses and cost reduction are crucial for industrial motor drives, hence an investigation about optimal chipset is required. Tandem FWD pair has been proposed as an interesting chipset solution in parallel with standard 1200 V IGBT technology due to low reverse recovery losses coefficients from 650 V diodes technologies. An analysis of different chipset technologies demonstrates that Si-based tandem FWD are potentially solutions bringing an equilibrated trade-off in cost and performance for standard motor drives applications limited by dv/dt values below 5 V/ns. Experimental results validated the proposed investigation.

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I. Introduction

Standard industrial motor drive applications commonly use the standard sixpack topology and 1200 V Si-based chipsets (IGBT + FWD) at switching frequencies up to 16 kHz – Figure 1. To avoid partial discharge phenomena or early insulation failures, variable speed motor drives without filtering between the converter and the motor must restrict voltage slope transitions to $3 \sim 5$ V/ns to reduce dv/dt stress on the machine windings [1], [2], [3].

While investigating chipset technologies capable of reliably and cost-effectively meeting these technical specifications, tandem diode solutions emerged as a preeminent alternative to the standard 1200 V FWD. In the tandem diode configuration, two 650 V diodes are connected in series (Figure 1.b), with the anode of one diode connected to the cathode of the other, considering snubber-less implementation. Hypothetically, this could guarantee safe commutation during transients and symmetrical voltage division in steady state and a low cost of implementation. Moreover, tandem diode components typically have lower reverse recovery loss coefficients than a standard Si-based 1200 V FWD.

Connecting FWD devices in series raises questions pertaining to the behavior of each individual device, particularly regarding voltage sharing in the blocked state and power losses during conduction and switching [4], [5]. Additional questions concern the reliability of series-connected diode systems as well as strategic considerations when using this type of configuration [1].

The proposed paper address these concerns and demonstrates key features of sixpack topologies using tandem FWD devices in combination with standard Si-based 1200 V IGBTs. The analysis focuses on industrial applications such as variable speed motor drive systems with dv/dt slopes in the range of $3 \sim 5$ V/ns and switching frequencies up to 16 kHz.

II. Semiconductor Power Losses for Motor Drive Systems

Generally, semiconductor power losses in the converter fall into two categories: switching and conduction losses. Conduction losses, also referred to as static losses, occur when power devices operate in saturation mode. Switching losses, often referred to as dynamic losses, happen as the device transitions between the blocking and conducting states.

Several approaches have been described to predict power losses in the standard sixpack topology. The proposed paper extends these to account for additional implications caused by connecting diodes in series, revealing both instantaneous and average power losses.

A. Modeling Instantaneous Static Losses

The instantaneous conduction losses of an IGBT p_{cond}^{IGBT} and a diode p_{cond}^{FWD} are a function of the collector-emitter current of the IGBT i_{ce}, the device current of the diode i_T, the collector-emitter voltage of the IGBT u_{ce} and the forward voltage of the diode u_T according to the following equation:

$$p_{cond}^{IGBT} = i_{ce} \cdot u_{ce}(i_{ce}, T_j^{IGBT}) \tag{1}$$

$$p_{cond}^{FWD} = i_T \cdot u_T(i_T, T_j^{FWD}) \tag{2}$$

The collector-emitter voltage of the IGBT u_{ce} and the forward voltage of the diode u_T depend on the device junction temperature T_j and the device currents i_{ce} and i_T. Datasheets provided by chipset

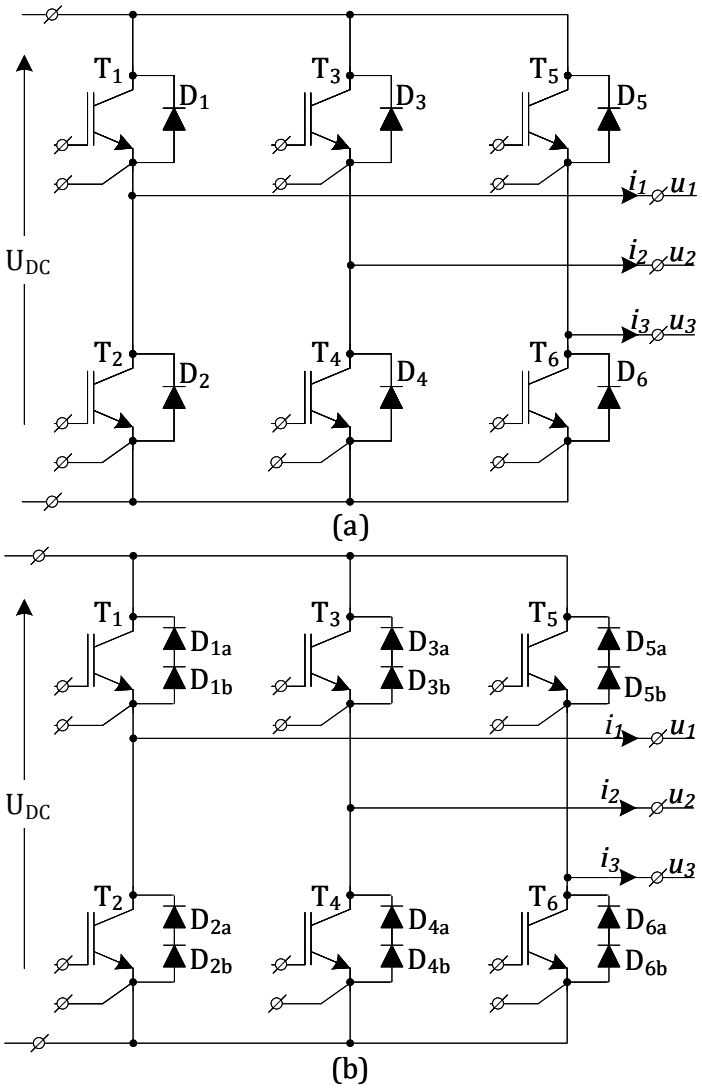

Fig. 1. Sixpack topologies used for standard motor drives system. (a) Sixpack topology implemented using a 1200 V Si-Based IGBT and a 1200 V FWD. (b) Sixpack topology implemented using a 1200 V Si-Based IGBT and tandem FWD (two 650 V devices in series).

suppliers typically list temperature-dependent offset voltages $U_{ce,0}$ and U_T and ohmic resistances R_{ce} and R_T. These can be used to estimate the device voltage during conduction. The resulting forward voltage equations of the IGBT and the diode are given by:

$$u_{ce}(i_{ce}, T_j^{IGBT}) = U_{ce,0}(T_j^{IGBT}) + R_{ce}(T_j^{IGBT}) \cdot i_{ce} \tag{3}$$

$$u_T(i_T, T_j^{FWD}) = U_T(T_j^{FWD}) + R_T(T_j^{FWD}) \cdot i_T \tag{4}$$

It is important to model the temperature dependency of the conduction loss model coefficients in (3) and (4). Most datasheets provide the forward voltage characteristics of the devices at 25°C and 125°C, making it possible to determine the conduction loss model coefficients $U_{ce,0}$, U_T, R_{ce}, and R_T for these temperatures and, by interpolating between these values, approximate their temperature dependency. Consequently, the device voltage u_{ce} and, by extension, the conduction losses of the IGBT and the diode can be estimated at any operation point.

For the tandem diode setup, devices $D_{x,A}$ and $D_{x,B}$ combine to form an equivalent diode and equation (4) becomes:

$$u_T(i_T, T_j^{FWD,eq}) = \\ U_{T,A}(T_j^{FWD,A}) + R_{T,A}(T_j^{FWD,A}) \cdot i_T \\ + U_{T,B}(T_j^{FWD,B}) + R_{T,B}(T_j^{FWD,B}) \cdot i_T \tag{5}$$

Next, the loss model should include the load phase current i_x ($x \in 1, 2, 3$) and the duty-cycle d. In a sixpack circuit, when the load current is positive ($i_x > 0$), the high-side IGBT and the low-side diode conduct the load current. During each switching period T_{sw}, the current first flows through the upper IGBT for a time interval $d \cdot T_{sw}$ and then through the lower diode for $(1 - d) \cdot T_{sw}$. Meanwhile, the conduction losses in the two other devices remain zero. When the current direction is reversed ($i_x < 0$), losses are incurred in the upper diode and the lower IGBT, while the other two devices do not experience any conduction losses.

B. Modeling Averaged Static Losses

The instantaneous conduction loss model is used as the basis for the development of an averaged conduction loss model for the tandem diode setup, which extracts the averaged loss over one electrical excitation T_1 (fundamental component). The averaged conduction loss model is obtained by assuming an ideal sinusoidal current and integrating over one excitation period T_1 of the load current.

$$P_{\text{losses,cond}}^{\text{IGBT,avg}} = \frac{1}{T_1} \int_{t=0}^{T_1} (U_{ce,0}(T_j) \cdot i_{ce} + R_{ce}(T_j) \cdot i_{ce}^2) dt \tag{6}$$

$$P_{\text{losses,cond}}^{\text{FWD,avg}} = \frac{1}{T_1} \int_{t=0}^{T_1} (U_T(T_j) \cdot i_T + R_T(T_j) \cdot i_T^2) dt \tag{7}$$

In the case for tandem FWD chipset (7) is modified to:

$$P_{\text{losses,cond}}^{\text{FWD,avg}} = \frac{1}{T_1} \int_{t=0}^{T_1} [(U_{T,A}(T_{j,A}) + U_{T,B}(T_{j,B})) \cdot i_T \\ + (R_{T,A}(T_{j,A}) + R_{T,B}(T_{j,B})) \cdot i_T^2] dt \tag{8}$$

C. Analysis on static losses parameters

To obtain dimensionless factors for the current stress acting on the power semiconductor devices, the following method is introduced: For a three-phase converter (Figure 1) supplying a standard three-phase motor, the modulation index (M) defines the transfer ratio between the DC-link voltage u_{dc} and the RMS value (fundamental component) of the phase voltage u_1.

$$M = \frac{2\sqrt{2} \cdot u_1}{u_{dc}} \tag{9}$$

Considering conventional carrier-based modulation scheme, the modulation function for the sixpack topology is given by:

$$d = \frac{1}{2} + \frac{M \cdot \sin(\omega_1 \cdot t)}{2} \tag{10}$$

The average (AVG) and RMS values of the normalized current stress acting on the IGBT and FWD can be calculated using the duty cycle d and the modulation index M as described below, where φ is the phase-shift angle and I_x is the RMS value (fundamental component) of the phase load current. Assuming

ideal symmetrical conditions and ignoring inductor phase current ripple, the current stress for the IGBT and FWD can be estimated as:

$$\frac{I_{cond}^{IGBT,avg}}{I_x} = \frac{1}{\pi\sqrt{2}}\left(1 + \frac{M \cdot \pi \cdot cos(\varphi)}{4}\right) \tag{11}$$

$$\frac{I_{cond}^{FWD,avg}}{I_x} = \frac{1}{\pi\sqrt{2}}\left(1 - \frac{M \cdot \pi \cdot cos(\varphi)}{4}\right) \tag{12}$$

$$\left(\frac{I_{cond}^{IGBT,rms}}{I_x}\right)^2 = \frac{1}{\pi}\left(\frac{\pi}{4} + \frac{2 \cdot M \cdot cos(\varphi)}{3}\right) \tag{13}$$

$$\left(\frac{I_{cond}^{FWD,rms}}{I_x}\right)^2 = \frac{1}{\pi}\left(\frac{\pi}{4} - \frac{2 \cdot M \cdot cos(\varphi)}{3}\right) \tag{14}$$

Since standard industrial motor drive systems operate in all four quadrants, the current stress in power devices must consider φ from 0 up to π rad. For a modulation index $M = 1$, the normalized current stress curves are presented in Figure 2, considering a phase shift φ from 0 to π rad (power factor from 1 up to -1). Figure 3 presents for the case for M= 0.5.

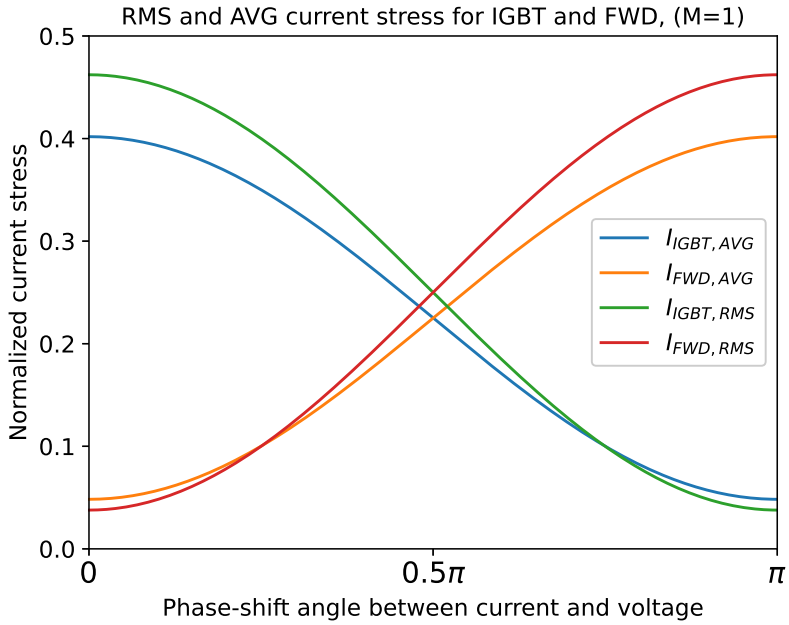

Fig. 2. Normalized current stress in IGBT and FWD in function of phase–shift angle between current and voltage, considering M=1.

Additionally, Figure 4 depicts the current stress for the IGBT/FWD as a function of the modulation index and considering a zero degree phase shift (PF=1). When the modulation index is zero, the current stress is similar for both the FWD and the IGBT. As the modulation index M increases, the current stress on the IGBT increases as well. The behavour is the same for conventional or tandem FWD sixpack topologies.

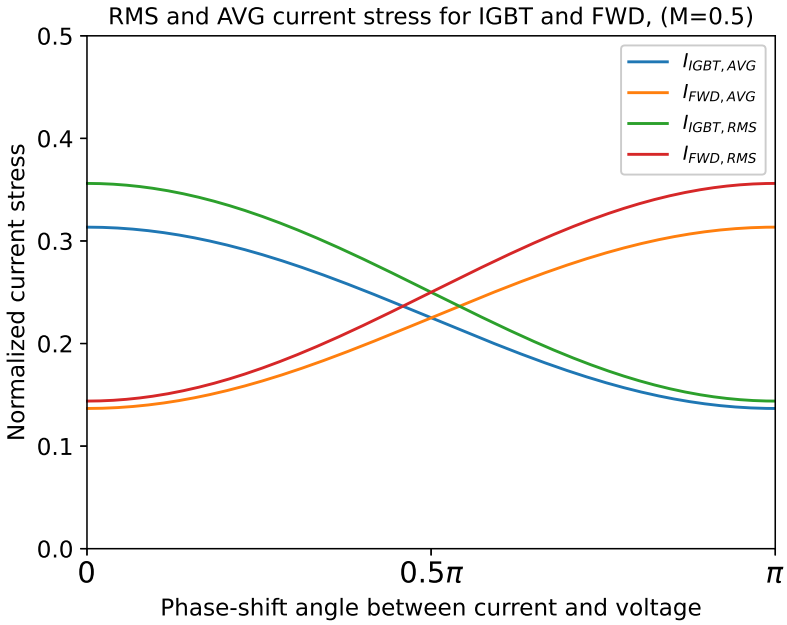

Fig. 3. Normalized current stress in IGBT and FWD in function of phase–shift angle between current and voltage, considering M=0.5.

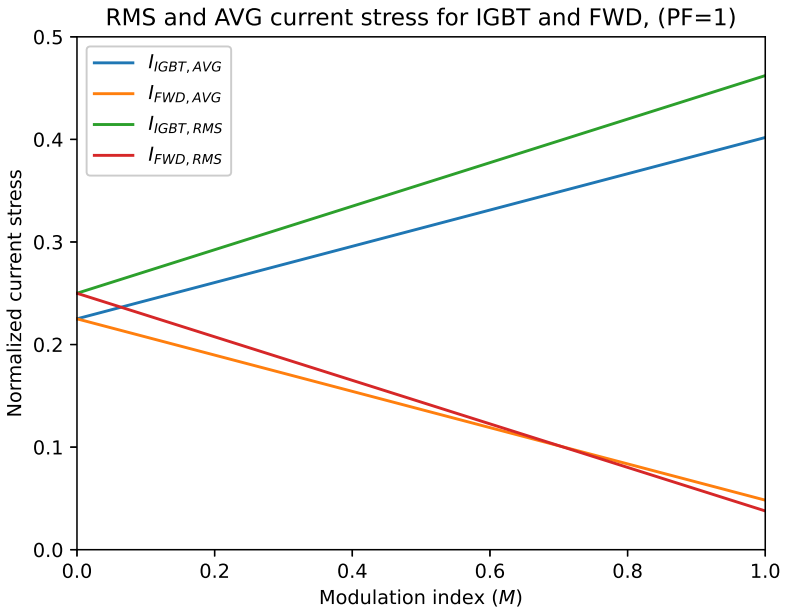

Fig. 4. Normalized current stress in IGBT and FWD in function of modulation index V, considering PF=1.0.

D. Modeling Instantaneous Dynamic Losses

Switching loss models for IGBTs assume that the switching loss energies grow nearly linearly with the load current. Switching losses in the IGBT depend on the gate resistance R_g and the dc-link voltage u_{dc}. The resulting model is given by:

$$E_{sw}^{IGBT} = E_0 + K_0 \cdot i_{ce} \cdot \frac{u_{dc}}{u_{dc}^{ref}} \cdot \frac{R_g}{R_g^{ref}} \tag{15}$$

$$E_{sw}^{FWD} = E_0^{rec}(u_{dc}) + K_0^{rec} \cdot i_T \cdot \frac{u_{dc}}{u_{dc}^{ref}} \cdot \frac{R_g}{R_g^{ref}} \tag{16}$$

The offset energy loss E_0^{rec} is typically a voltage dependent property and can be described by the following equation:

$$E_0^{rec}(u_{dc}) = E_0^{rec}(u_{dc}^{ref}) \frac{u_{dc}}{u_{dc}^{ref}} \tag{17}$$

The introduced model can be used to estimate the switching loss energies of IGBTs and diodes. The total switching losses of the devices $P_{sw,loss}^{IGBT}$ and $P_{sw,loss}^{FWD}$ depend on their switching loss energies E_{sw}^{IGBT} and E_{sw}^{FWD} and the switching frequency of the converter f_{sw}:

$$P_{sw,loss}^{IGBT} = E_{sw}^{IGBT} \cdot f_{sw} \tag{18}$$

$$P_{sw,loss}^{FWD} = E_{sw}^{FWD} \cdot f_{sw} \tag{19}$$

In the case of tandem FWD chipset, the single modification is the reverse recovery coefficients that should be update in order to find $P_{sw,loss}^{FWD}$.

E. Modeling Averaged Dynamic Losses

The presented switching loss model allows to estimate switching losses incurred by the devices at every switching period. However, for many applications, the averaged switching losses over an excitation period of the current T_1 are of interest. The following shows how the loss model can be used to predict the averaged losses over one fundamental period of a sinusoidal load current.

For this, the switching losses of the diode and the IGBT, derived in (18) and (19), must be integrated over one period of the load current.

$$P_{\text{losses,sw}}^{\text{IGBT,avg}} = \int_{t_0}^{t_0+T_1} p_{sw}^{IGBT}(i_{ce}, T_J^{IGBT}, u_{dc}, R_g)dt \tag{20}$$

$$P_{\text{losses,sw}}^{\text{FWD,avg}} = \int_{t_0}^{t_0+T_1} p_{sw}^{FWD}(i_T, T_J^{FWD}, u_{dc}, R_g)dt \tag{21}$$

For tandem FWD setup, the coefficients for p_{sw}^{FWD} prediction will consider the impact of both devices ($D_{x,A}$ and $D_{x,B}$). Hence, the average value of dynamic losses can be determined from the integration of instantaneous power p_{sw}^{FWD} during a period of fundamental component f_1.

F. Analysis of dynamic losses parameters

The reverse recovery process is defined by diode capacitive effects which impact the reverse recovery characteristics [6]. The typical FWD current and voltage waveforms during the reverse recovery phenomenon are demonstrated in Figure 5.

The typical diode commutation starts with the application of the reverse voltage on device ($t = t_0$). The current falls at a rate $-di_T/dt$ up to reaches the zero crossing point ($t = t_1$). This phase is dependent on the circuit components, since $-di_T/dt$ is function of the reverse voltage, parasitic inductance and the IGBT gate-circuit circuit configuration (gate resistor, gate voltage and so on). When the i_T current turns negative ($t = t_1$), hence starts storage phase up to instant that total excess carrier concentration reduced to zero ($t = t_2$). After t_2 voltage across the diode increases by a rate of $-du_T/dt$ until at that point di_T/dt=0 and the diode current reaches its peak value I_{RRM} ($t = t_3$). After that, voltage across the diode continue increasing by $-du_T/dt$ until it reaches the peak value V_{RRM} ($t = t_4$). The last phase starts when the voltage begins to fall achieving its steady state reverse blocking value at $t = t_5$, while the current continues to drop up to its leakage values.

Experimental measurements for the reverse recovered current are demonstrated in Figure 6. In this case, a benchmark between the standard FWD and tandem FWD results are highlighted in function of gate resistor. Substantial reduction on reverse recovery losses is achivied by using tandem FWD chipset.

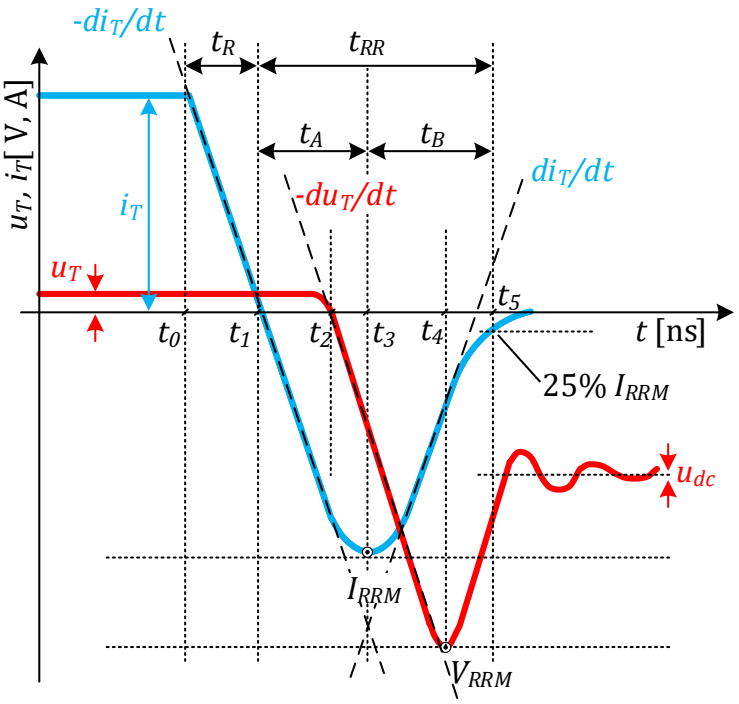

Fig. 5. Typical diode current and voltage waveforms during reverse recovery phenomenon.

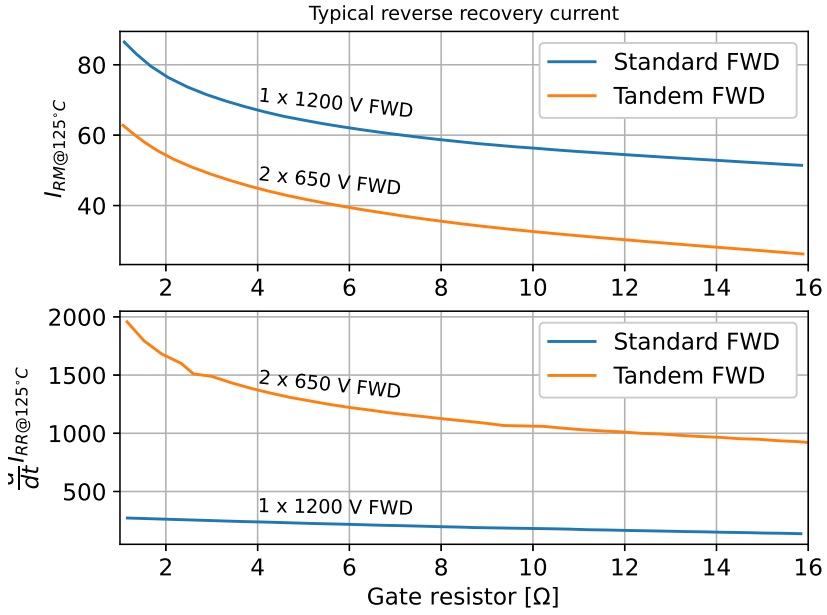

Fig. 6. Benchmark between different diodes chipset technologies for the reverse recovery current in function of gate resistor.

III. Chipset Power Losses Benchmark Analysis

Extended power losses analysis has been investigated considering power modules implementation. The products have been selected considering same IGBT technology, housing and DBC substrates. The single difference between them are the FWD chipset [7]. The partnumber are given by:

- Power Module **10-FY126TA050M7-L828F78**. It is composed by standard IGBT M7 with Tandem FWD

- Power Module **10-FY126PA050M703-L828F03**. It is assembled with standard IGBT M7 and standard FWD.

TABLE I
OPERATION CONDITIONS

Parameter	Value
dc-link voltage	$U_{dc} = 800$ V
load current RMS value	$I_x = 25$ A
load voltage RMS value	$U_x = 230$ V
load frequency (fundamental component)	$f_1 = 50$ Hz
Power factor (load phase-shift)	$PF = \pm 0.8$
Gate-Resitor (ON and OFF)	$R_g = 8\ \Omega$

The performance benchmark results are depicted in Figure 7, taking operation conditions parameters as demonstrated in Table I. Semiconductor power losses are reported for various chipset technologies considering switching frequencies commonly encountered in industrial motor drive systems and dv/dt values below 5 V/ns. Overall, the proposed Tandem FWD setup combined with a standard IGBT was found to exhibit lower losses compared to those with a standard 1200 V IGBT/FWD pair. While the static losses are slightly higher in the Tandem FWD setup, the minimization of dynamic losses more than compensates for this difference.

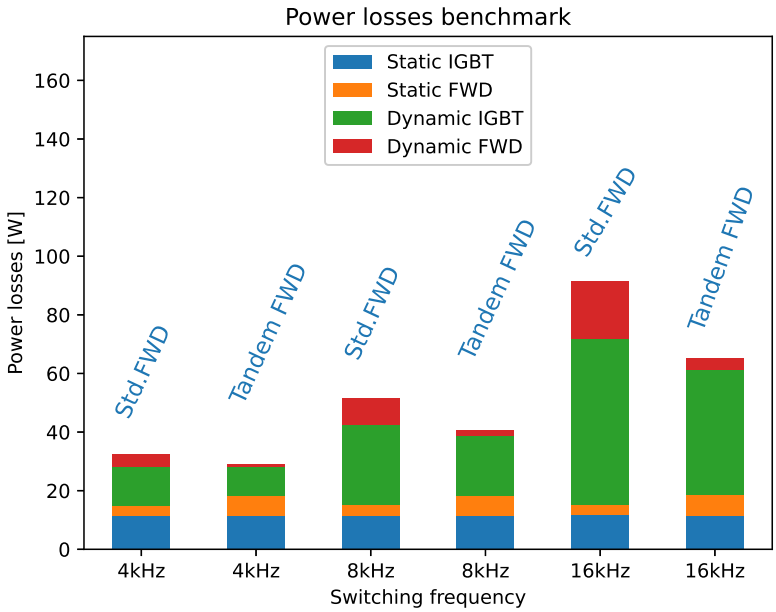

Fig. 7. Detailed description of semiconductor power losses for different chipset configurations operating at switching frequencies [4;8,16] kHz. Considering load phase-shift with PF 0.8 positive.

The Figure 8 demonstrates results for similar analysis, nevertheless with power factor negative ($PF = -0.8$). As demonstrated in Figure 2 and Figure 3, the FWD are overstressed during negative power factor, impacting static losses. Nonetheless, the results demonstrated in Figure 8 indicate that the tandem FWD has similar losses in overal even operating during this load conditions.

Consequently, at the same system-level current and operating conditions, the sixpack topology with tandem diodes outperforms the conventional sixpack circuit, and its advantage increases with the switching frequency. The main reason is that tandem FWD chipset has lower reverse recovery coefficientes.

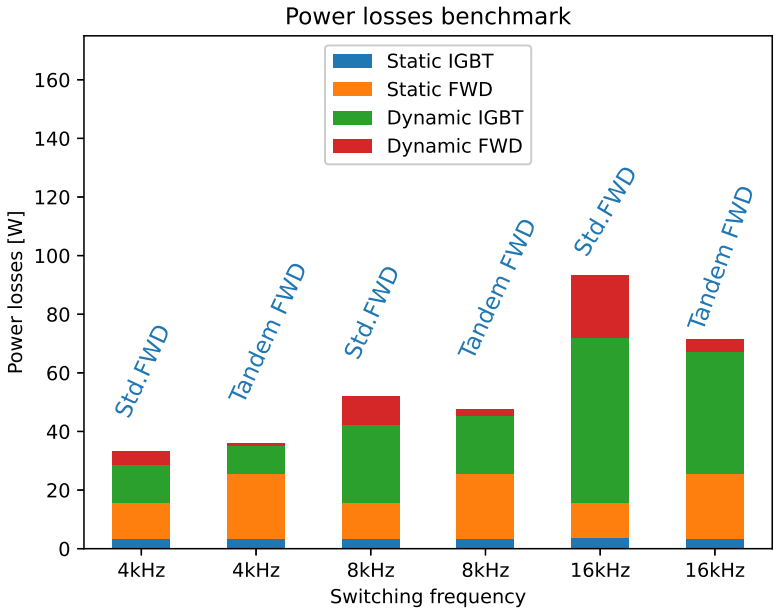

Fig. 8. Detailed description of semiconductor power losses for different chipset configurations operating at switching frequencies [4;8,16] kHz. Considering load phase-shift with PF 0.8 negative.

Therefore, implementations with tandem diodes are recommended for sixpack topologies operating at higher switching frequencies, than standard values often used in industrial applications such as motor drive systems.

IV. Conclusion

Tandem diodes offer a promising solution for 1200 V chipsets used in a range of industrial motor drive applications. By reducing dynamic losses and increasing efficiency, these devices can help engineers to create more reliable and energy–efficient power conversion systems. The proposed investigation demonstrates the power loss reduction provided by Tandem FWD solutions when comparing against conventional 1200 V IGBT-FWD pair devices. Experimental results obtained using a double pulse measurement setup corroborate the proposed analysis, demonstrating a significant reduction of semiconductor power losses which significantly improve the system lifetime at an affordable cost.

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